AD-A058 609 HONEYWELL INC ST PETERSBURG FL AVIONICS DIV F/G 9/5
MANUFACTURING METHODS AND TECHNOLOGY ENGINEERING FOR TAPE CHIP --ETC(U)
AUG 78 W R DE MIRANDA DAAB07-77-C-0526

UNCLASSIFIED DELET-TR-77-0526-3 NL

1 OF 1

AD
A058609

END
DATE
FILMED
11-78
DDC

LEVEL III

(13)

Research and Development Technical Report

DELET-TR-77-0526-3

AO53 088
AO49 179

MANUFACTURING METHODS AND TECHNOLOGY Engineering FOR TAPE CHIP CARRIER

William R. Rodrigues de Miranda
Honeywell Inc.
St. Petersburg, Florida 33733

August 1978

Quarterly Report for Period Ending 31 March 1978

(Approved for Public Release - Distribution Unlimited)

PREPARED FOR

Electronics Technology and Devices Laboratory

ERADCOM

US ARMY ELECTRONICS RESEARCH AND DEVELOPMENT COMMAND
FORT MONMOUTH, NEW JERSEY 07703

CONTRACT NO. DAAB07-77-C-0526
HONEYWELL INC.
ST. PETERSBURG, FLORIDA 33733

NOTICES

Disclaimers

The citation of trade names and names of manufacturers in this report is not to be construed as official Government indorsement or approval of commercial products or services referenced herein.

Disposition

Destroy this report when it is no longer needed. Do not return it to the originator.

19

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. ~~REPORT NUMBER~~
18 DELET-TR-77-0526-3

2. GOVT ACCESSION NO

3. RECIPIENT'S CATALOG NUMBER
no. 1

4. ~~TITLE (AND SUBTITLE)~~
6 Manufacturing Methods and Technology Engineering for Tape Chip Carrier.

5. ~~TYPE OF REPORT & PERIOD COVERED~~
9 Quarterly Report, 1 Jan - 31 Mar[redacted]78,

6. ~~PERFORMING ORG.~~ REPORT NUMBER

7. AUTHOR(s)
10 William R. Rodrigues de Miranda

8. CONTRACT OR GRANT NUMBER(s)
15 DAAB 07-77-C-0526

9. PERFORMING ORGANIZATION NAME AND ADDRESS
Honeywell Inc., Avionics Division 393 215
13350 US Highway 19
St. Petersburg, FL 33733

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
17 C2
16 IL762705AH94 C2 200

11. CONTROLLING OFFICE NAME AND ADDRESS
ERADCOM
ATTN: DELET-IT
Fort Monmouth, NJ 07703

12. ~~REPORT DATE~~
June 1978 11 Aug 78

13. NUMBER OF PAGES
60

14. MONITORING AGENCY NAME AND ADDRESS (IF DIFFERENT FROM CONTROLLING OFFICE)

15. SECURITY CLASS. (OF THIS REPORT)
Unclassified 12 69p.

15A. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A

16. DISTRIBUTION STATEMENT (OF THIS REPORT)

Approved for Public Release - Distribution Unlimited

17. DISTRIBUTION STATEMENT (OF THE ABSTRACT ENTERED IN BLOCK 20, IF DIFFERENT FROM REPORT)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (CONTINUE ON REVERSE SIDE IF NECESSARY AND IDENTIFY BY BLOCK NUMBER)

Tape Chip Carrier
Hybrid Microcircuit
Film Carrier
Inner Lead Bonding
Outer Lead Bonding
Automatic Feed Mechanism
Material Handling System
Automatic Assembly Line

20. ABSTRACT (CONTINUE ON REVERSE SIDE IF NECESSARY AND IDENTIFY BY BLOCK NUMBER)

This report describes the work performed during the first quarter of a 26-month contract. The contract is aimed at establishing and demonstrating the feasibility of an automated assembly line for hybrid microcircuits using tape chip carrier technology for semiconductor devices whenever practical. The automated line will also make use of automatic substrate handling equipment to move partially assembled devices in and out of magazines.

393 215

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

INTRODUCTION

The purpose of this program is to demonstrate the concept of an automated assembly line for hybrid microcircuits, through the establishment of techniques for tape carrier mounting of semiconductor chips, burn-in and testing of these chips on tape and their placement into representative hybrid circuits. The Tape Chip Carrier (TCC) system permits mounting of semiconductor chips on reels of sprocketed film The system is an established means of automating the interconnection of individually packaged semiconductor chip devices. It has been adapted to the fabrication of hybrid microcircuits used in the manufacture of certain commercial computers. The Army is interested in utilizing the tape carrier mounting technology for the manufacture of hybrid microcircuits for military electronic applications when advantageous for economic reasons or desirable from the viewpoint of increased reliability. Its overall adaptation to the hybrid microcircuit industry is expected to be greatly enhanced by this program. The automated assembly line will make use of an automatic feed mechanism at each process step, and magazines to transport substrates and partially assembled circuits between process points.

This is the third quarterly report on the MM&T program. Honeywell is pleased to report continued excellent progress as the program moved into the Tape Chip Carrier phase.

SECTION 1

EQUIPMENT

This task covers the evaluation of existing, in-house equipment for possible use for the MM&T tasks to be performed, and the review of requirements and preparation of specifications for equipment to be purchased. After review, a number of changes were made to the earlier planned equipment listed on the PERT chart (CDRL-A001, August 1977) for the sake of scheduling and cost effectiveness. Each of the equipment items now planned will be discussed further.

A. REEL-TO-REEL PLATER

After considerable experience with the Honeywell designed tape plating facility, now fully operational in our plant (See Figure 1-1) it became apparent that sufficient capacity exists to support the Confirmatory Sample and Pilot Line phases of the program. The current output rate is 1,600 frames per eight hour shift with near 100 percent yield. Although this plater can handle only 12 inch strips, it is felt that in order to demonstrate inner lead bonding (ILB) production rates on the automatic bonder (the only place where continuous tape is required) the strips can be spliced with the aid of a simple splicing device.

A special fixture, also developed by Honeywell allows savings of up to 60 percent in gold as it selectively plates the test pad area with a protective flash only, while plating the gold on the used lead frame area with the required 130 microinches thickness (See also Figure 1-1).

B. AUTOMATIC WIRE BONDER

The purchase specifications and purchase requisitions for a K&S[1] Model 1415-3 Automatic Wire Bonder have been prepared and will be released during the next reporting period. The machine will be purchased without the automatic pattern recognition feature. This device can be added later if experience with the machine in the automatic feed mode shows that it will materially improve the rate and performance.

C. DIE PLACEMENT AND EPOXY DISPENSER

After careful review a decision has been made not to automate the die placement function for transistor dice. The equipment proposed by K&S is not yet fully developed and would require significant lead time. Performance would even then be unproven. Furthermore the die index

---

1 Kulicke & Soffa (K&S) Inc., Prudential Road, Horsham, PA 19044

A7802-034

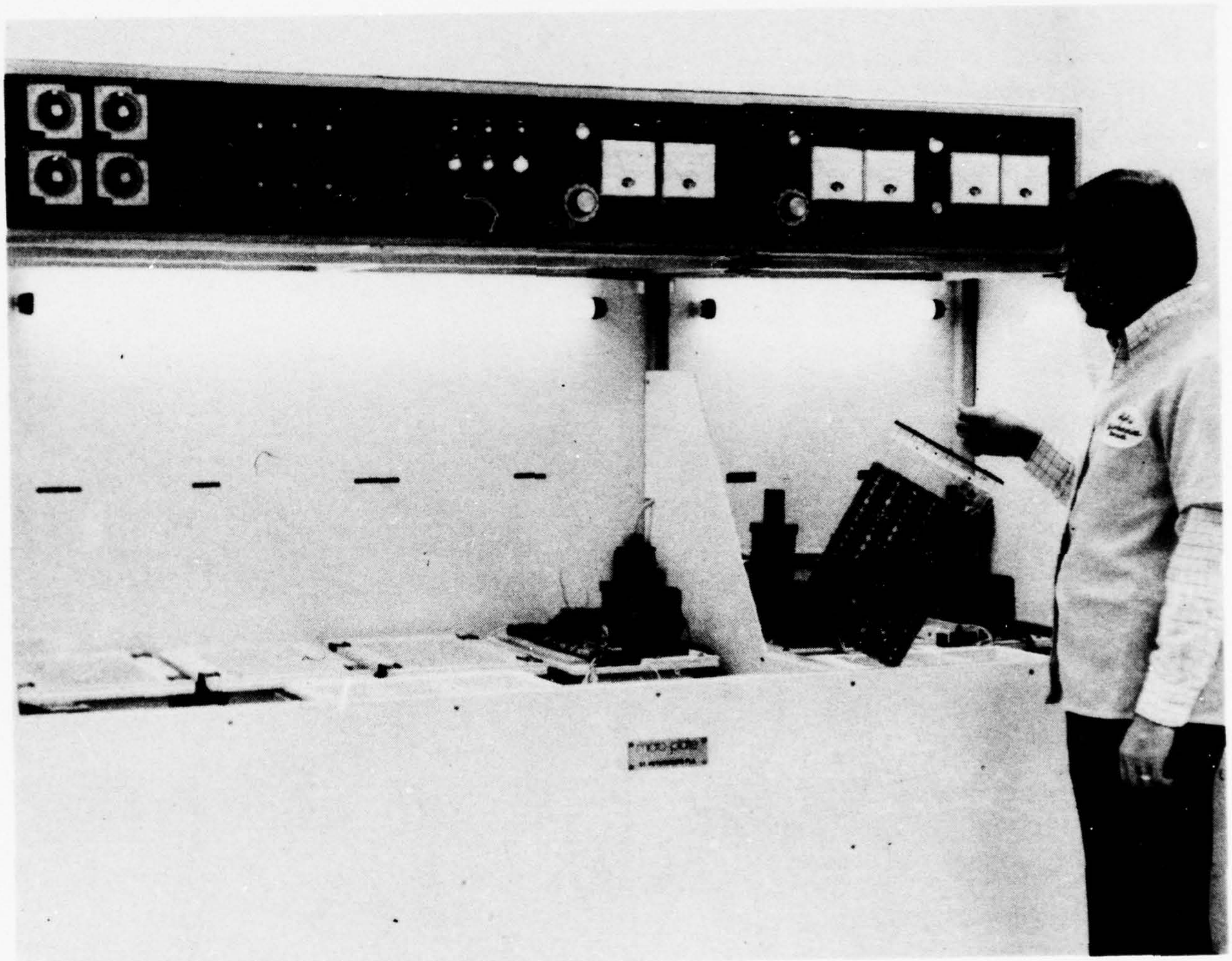


FIGURE 1-1. HONEYWELL DESIGNED TAPE PLATER
AND HALDEY FIXTURE

function would not be automated. It was therefore decided that while the IC die placement is done automatically at the time of outer lead bonding, the discrete device dice should be placed with in-house manual equipment. This equipment has a placement rate of 180 per hour, more than adequate match the production rate requirements for the specified operation.

D. TAPE INSPECTION EQUIPMENT

The in-house tape inspection equipment consisting of a manual spooler/dispooler with a Bausch and Lomb stereo 7 microscope has been deemed adequate to meet the requirements for the program through the Confirmatory Sample phase. A method to inspect for alignment defects prior to automatic inner lead bonding will be investigated.

E. OUTER LEAD BONDER - FRAMER

During the remainder of the Engineering Sample phase and during the Confirmatory Sample phase the framing operation can be performed manually as has recently been demonstrated. The automatic framing equipment is now scheduled to be ordered in January 1979. However, if necessary the automatic framing operations for the Pilot Line phase may be run on automatic equipment currently available in Honeywell's LISD facility in Phoenix, Arizona.

F. OUTER LEAD BONDER - TESTER/CODER

The tester coder equipment specifications have been prepared and the purchase requisition will be released during the next reporting period.

G. OUTER LEAD BONDER - COMPOSER

Because of the relatively small quantity of different IC chip types per hybrid (14 for the most complex case) the composing function can be accomplished manually during both Engineering and Confirmatory Sample phases. The automatic Composer will be ordered in January 1979. If necessary the Composing equipment available in Honeywell's LISD facility in Phoenix, Arizona can be used for production or demonstration purposes.

H. OUTER LEAD BONDER - ASSEMBLER

The automatic assembler specifications have been prepared and the purchase requisition will be released during the next reporting period.

I. INNER LEAD BONDER

The Automatic Inner Lead Bonder will be a standard Model 1-1000 Jade machine. The appropriation for the machine will be completed during the next reporting period. Several of the items of optional equipment to be included with the order are listed below.

- 15-inch diameter reel and dereel system with environmental chambers.
- Precision Manual sample punch
- ILB Thermode planarity adjustable system
- Variable magnification system
- Objective lens for other field of view
- Dial Indicator assembly
- Inspection scope (Stereo-Wild M3) mounted with tool post
- ILB heated base with temperature controller.
- Adjustable post bond delay (0 - 2 sec)

SECTION 2

MATERIAL HANDLING SYSTEM

Two basically different types of automatic handling equipment have been developed: a mechanical handler and an air handler. (See previous reports). Both approaches proved satisfactory. As anticipated, the air handler is faster, cheaper, and more reliable than the mechanical handler. This air handler is now in the debugging phase. It will be used on the Weltek thick film printer. The mechanical handler will be adapted to the automatic wire bonder where the speed and reliability requirements are somewhat less rigorous than on the screen printer.

Four of our substrate processing machines employ belts for moving the substrates:

1. Furnace (four abreast)

2. Dryer (three abreast)

3. Solder reflow (one)

4. Capacitor assembler (one)

The automatic equipment for loading the belts from the magazines will be similar for all four machines. A mechanism indexes the magazine and sequentially loads substrates on a cross slide (See Figure 2-1). When the slide is loaded with the required number of substrates, (one, three, or four) they are moved, abreast, onto the belt machines.

An air sensor(s) locates the substrate(s) on the moving belt and triggers a vacuum arm that picks the substrate(s) off the belt and moves them to a cross slide that employs directed air jets to move them (See Figure 2-2) to the magazine load and index mechanism (See Figure 2-3).

Power for the belt loaders and unloaders is supplied by air cylinders. Control logic power is 24 volts dc. A technique to dry the substrates in the magazines in a special furnace is presently being evaluated as an alternative to building an automatic loader and an unloader for the conventional belt dryer. This appears to offer savings in equipment cost, space, run time, scrap, and maintenance. (This approach is not feasible for the furnaces or the solder reflow because of the high temperatures and tight controls required by these processes).

The following is a status summary of these and other equipment items of the Material Handling System. (See Figure 2-4 for the design and manufacturing schedule).

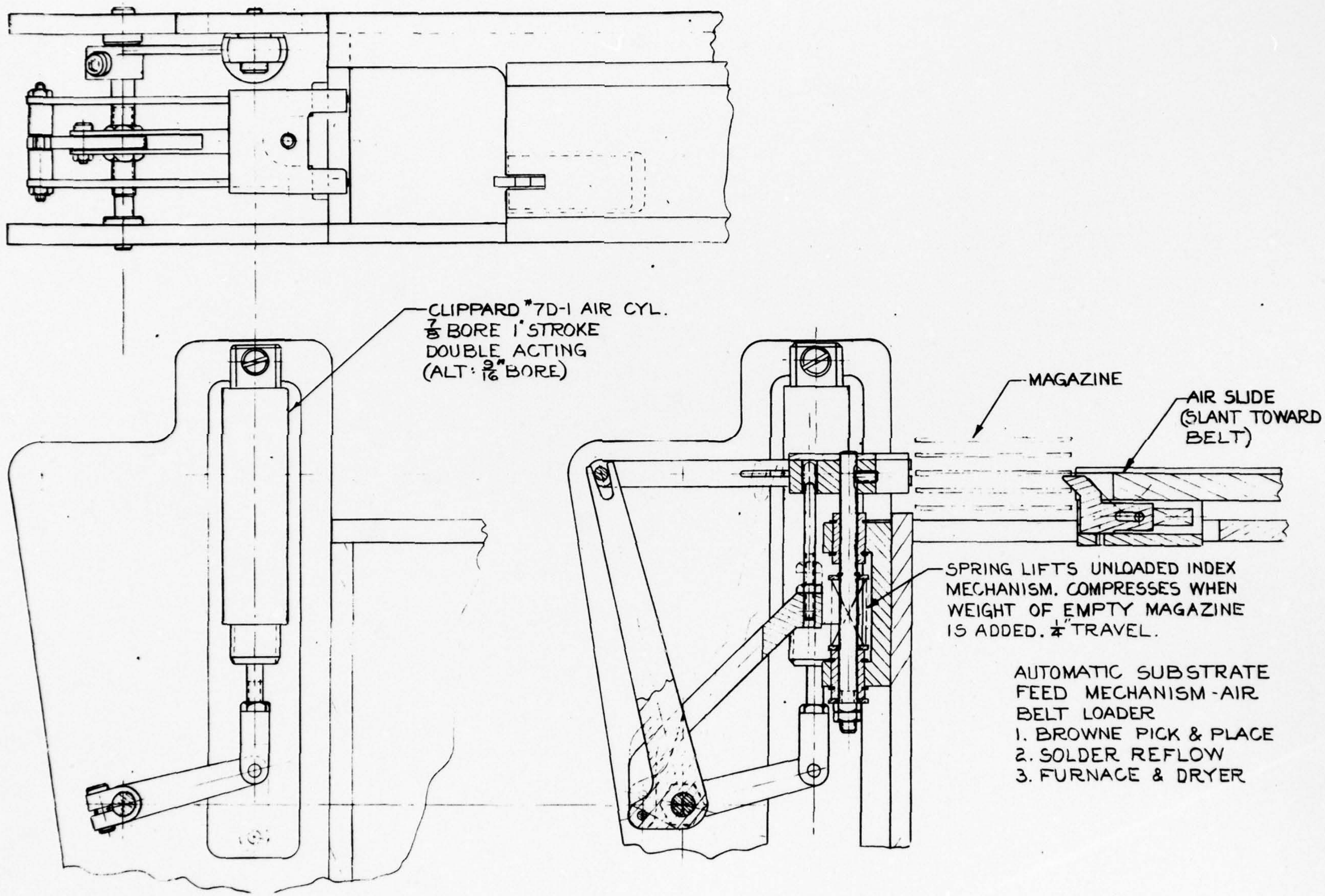


FIGURE 2-1. AUTOMATIC SUBSTRATE FEED MECHANISM - BELT LOADER

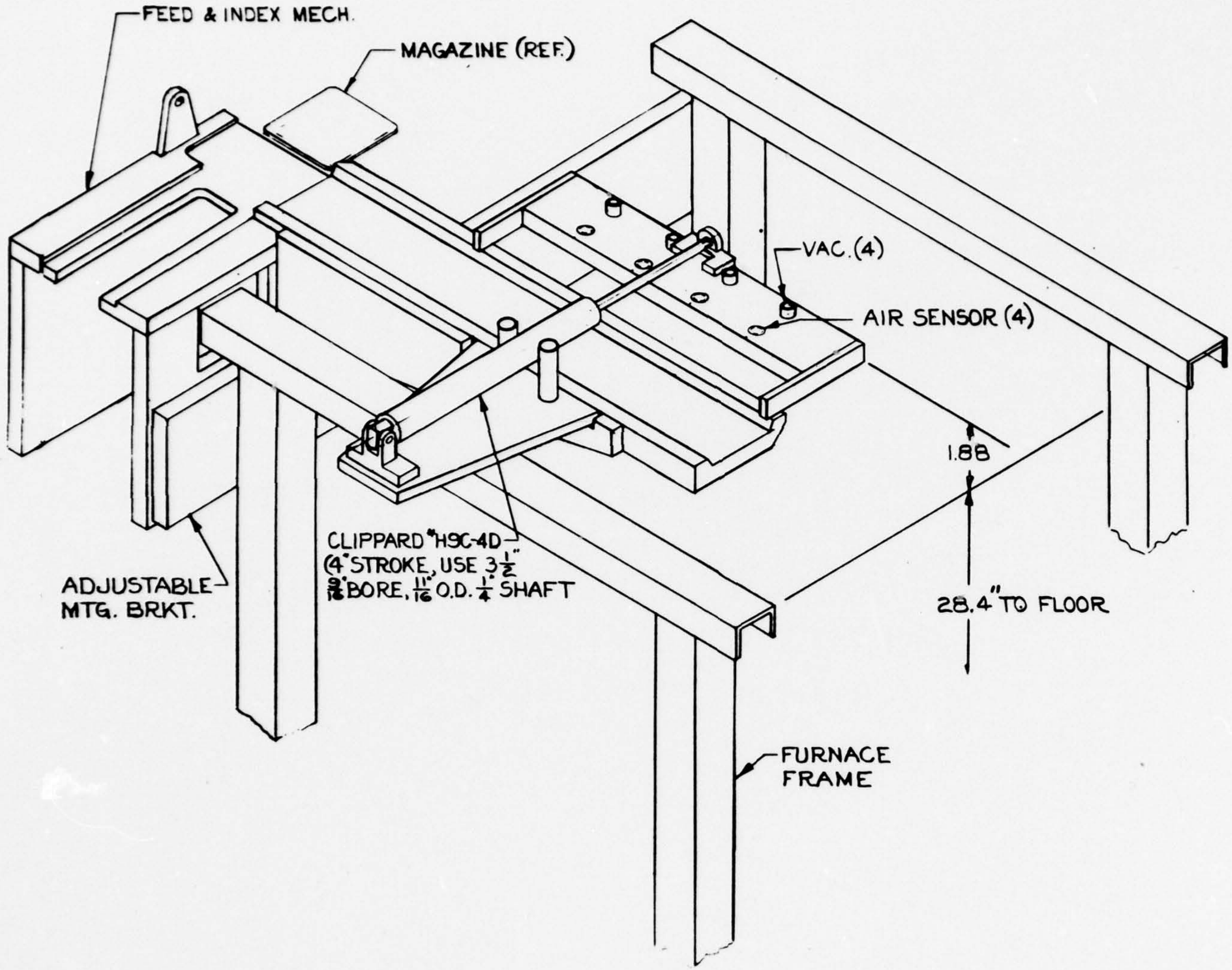


FIGURE 2-2. AUTOMATIC SUBSTRATE FEED MECHANISM - CROSS SLIDE

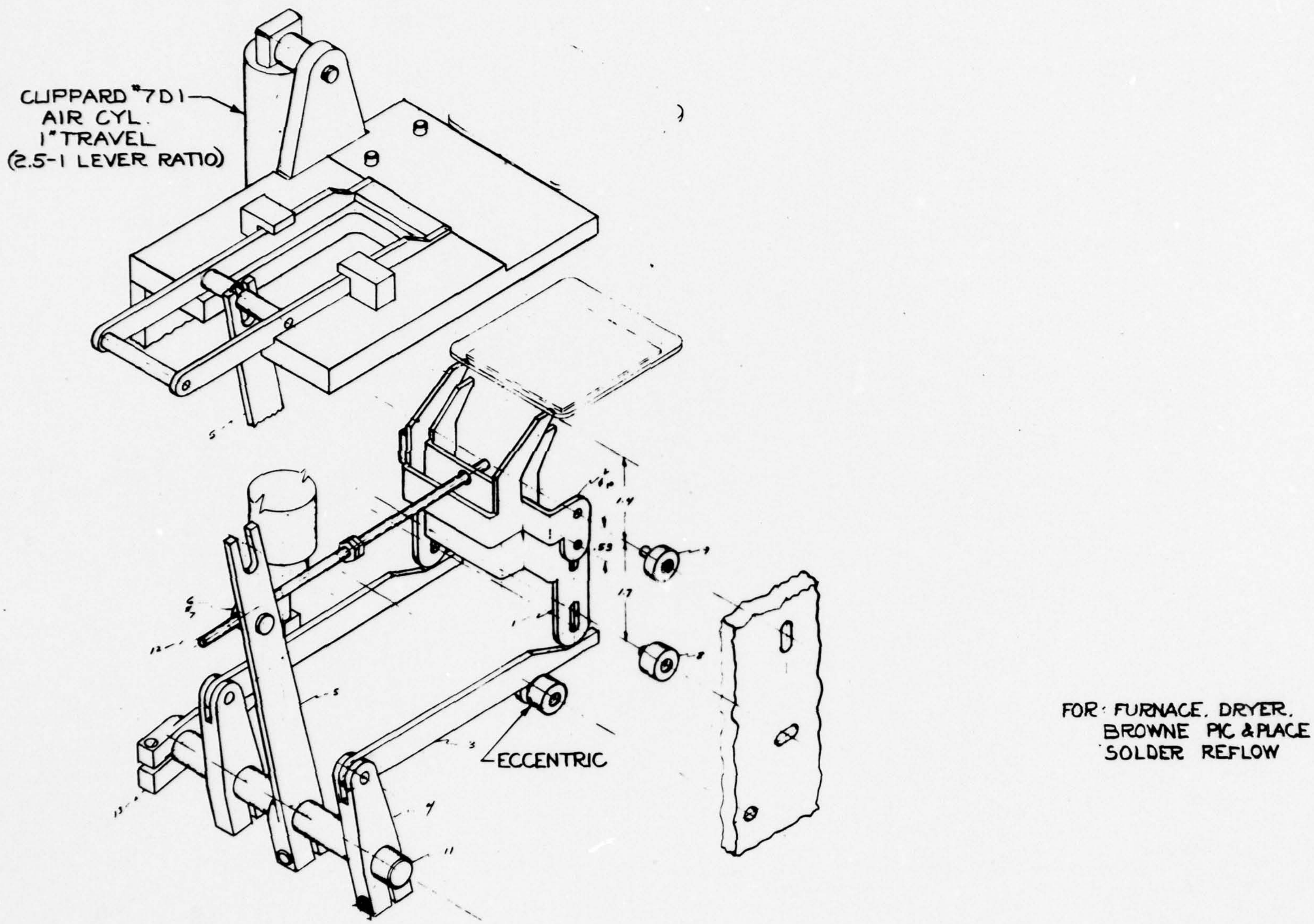


FIGURE 2-3. AUTOMATIC SUBSTRATE FEED MECHANISM - LOAD AND INDEX MECHANISM

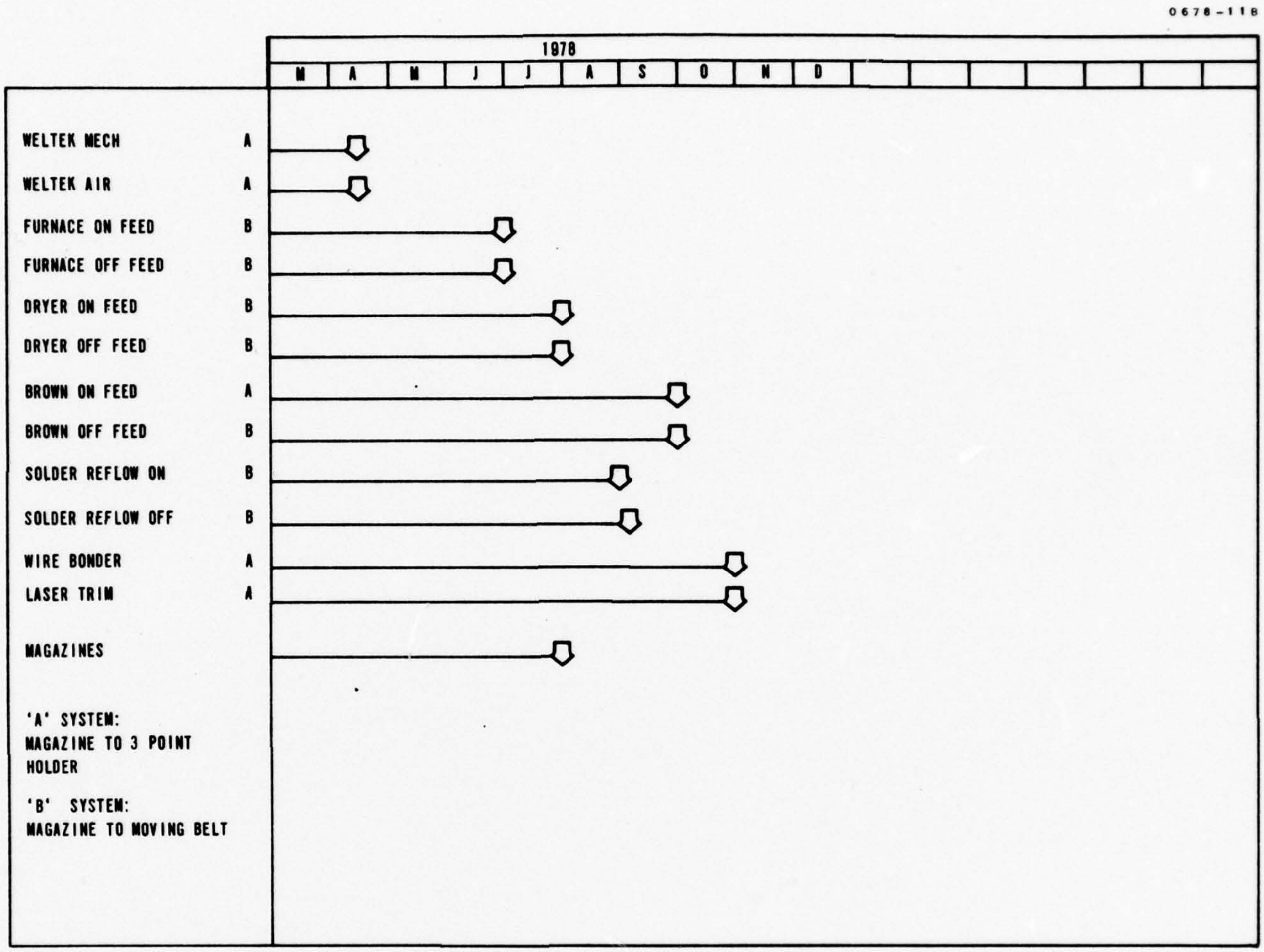


FIGURE 2-4. DESIGN AND MANUFACTURING SCHEDULE FOR MATERIAL HANDLING SYSTEM EQUIPMENT

1 - The Mechanical Substrate Handling System has been completed and married to the Weltek screen printer. The system is operational and has been successfully demonstrated several times. Several minor "bugs", mostly in the electronics system remain. Figure 2-5 shows a photograph of the system prior to mounting on the printer. Figure 2-6 shows a close-up of substrate track.

Plans: Remove system from Weltek and rebuild base only for use with Automatic Wire Bonder. Upgrade and debug electronics (need self-zeroing, cable shielding and improved packaging).

2 - The Air Substrate Handling System has been completely assembled but requires some debugging and rework to become operational. The basic operation has been demonstrated apart from the Weltek printer.

Plans: Rework and debug the system. Marry to Weltek, debug and demonstrate. Leave Air System on Weltek.

3 - The Furnace On-Loader has been completely assembled and was successfully demonstrated a number of times. Minor adjustments and electrical hook-up needs to be completed.

Plans: Marry the Furnace On-Loader to the Lindburg (9-inch belt) furnace, debug and demonstrate.

4 - Furnace Off-Loader design is 40 percent complete, build is 20 percent complete.

Plans: Complete and demonstrate with Lindberg furnace.

5 - Dryer On-Loader design is 90 percent complete. Build not started.

Plans: Complete design and build. Demonstrate on dryer.[1]

6 - Dryer Off-Loader design is 40 percent complete. Build not started.

Plans: Complete design and build. Demonstrate on dryer.[1]

7 - Browne On-Loader, Browne Off-Loader, Solder Reflow On-Loader, Solder Reflow Off-Loader: Design for all is 10 percent complete, build not started.

Plans: Complete design and build. Demonstrate on respective machines/equipment.

8 - Automatic Wire Bonder will be supplied with an automatic substrate handling system through modification of the Weltek mechanical feed system (See 1).

---

1 See text on page 2-1 for alternate plan.

A7802-037

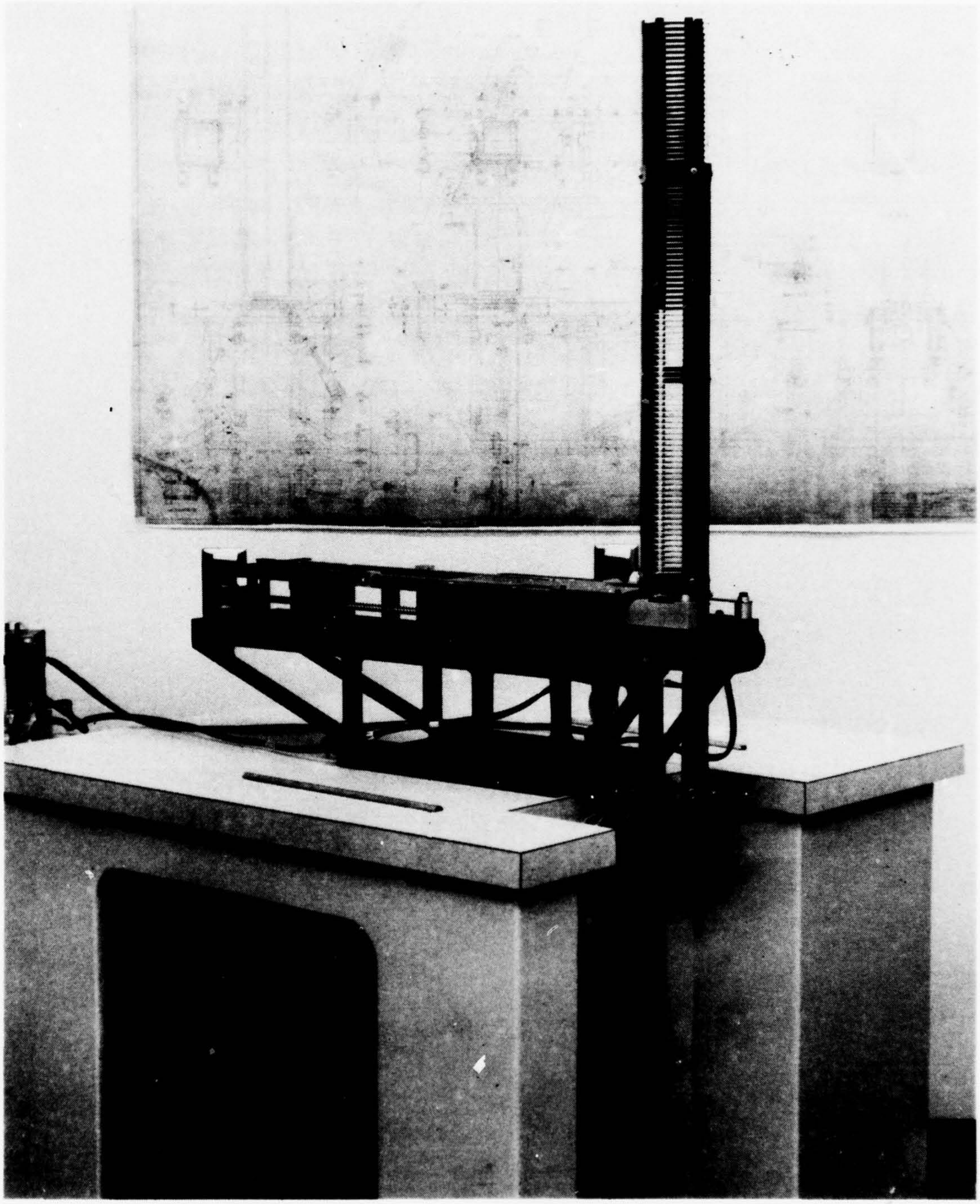


FIGURE 2-5. MECHANICAL SUBSTRATE HANDLING SYSTEM

A7802-038

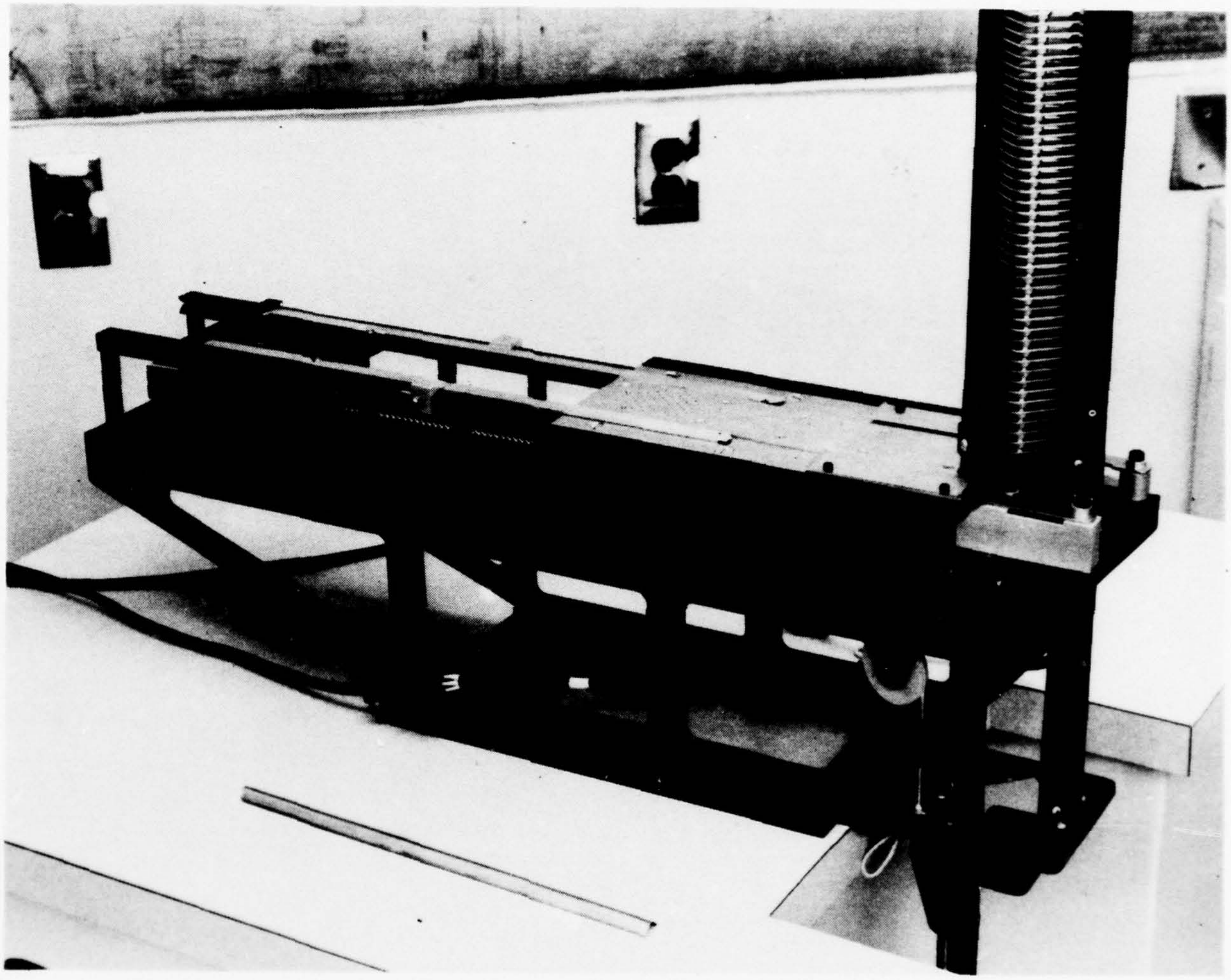


FIGURE 2-6. MECHANICAL SUBSTRATE HANDLING SYSTEM
CLOSE UP OF SUBSTRATE TRACK

9 - Laser Trim Equipment will be equipped with an automatic handling system similar to the Air Substrate Handling System currently being completed for the Weltek. Design for this system is 75 percent complete. Build has not yet started.

10 - Four Magazines are completed. Current plans include a total build of 30. Build of no other magazines has yet been started.

SECTION 3

BURN-IN ON TAPE

A. BURN-IN TANK

Design of the burn-in tank is proceeding on schedule. Heater pads, temperature controller, relays and printed wiring boards have been ordered. Purchased items are expected in-house by 14 July 1978.

Figure 3-1 shows a layout drawing of the tank. It is constructed of plate aluminum, with all pieces welded together for liquid-tight joints. While the tank is large enough to house ten trays, until the concept is proven only one tray will be installed. To accomplish this, a partition is welded inside at the fluid inlet end.

Heater pads are bonded to the four sides and bottom, as well as the internal partition. High temperature insulation covers all sides of the tank as well as the partition. Protection for the insulation is provided by thin sheet metal skins.

The burn-in fluid will be circulated through the tank by a pump. For this reduced capacity tank, a pump already in use on a similar program will be utilized. When the tank is expanded to full capacity, a larger pump will be obtained.

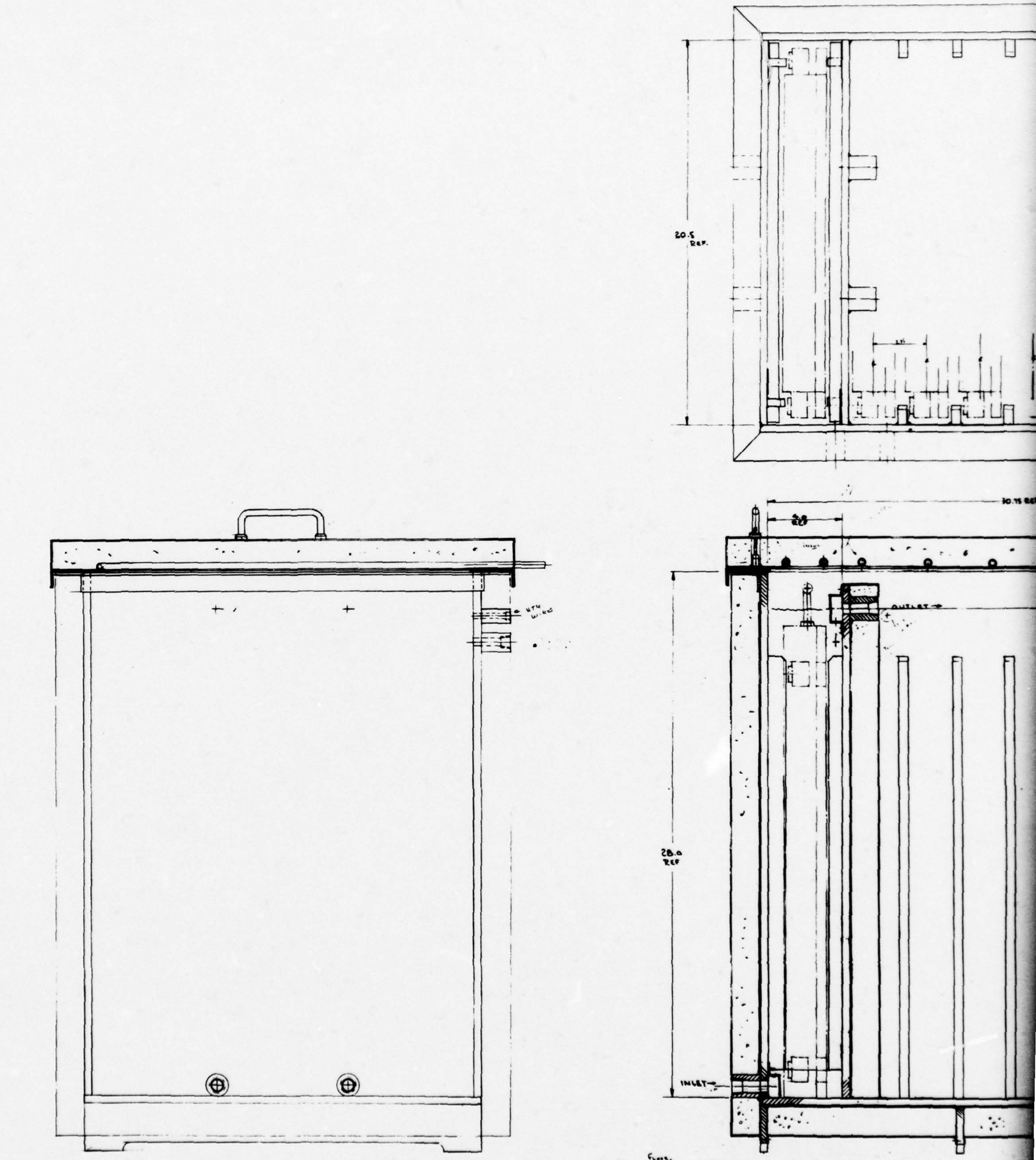
Temperature of the fluid in the tank will be maintained by a Fenwal Temperature Controller. In case of thermal runaway due to malfunction of the controller, an over-temperature sensor will de-activate the main power relay, shutting the system down.

Cold water circulating through tubing on the cover will minimize vapor losses by condensing vapors on the cover and condensate dripping back into the tank.

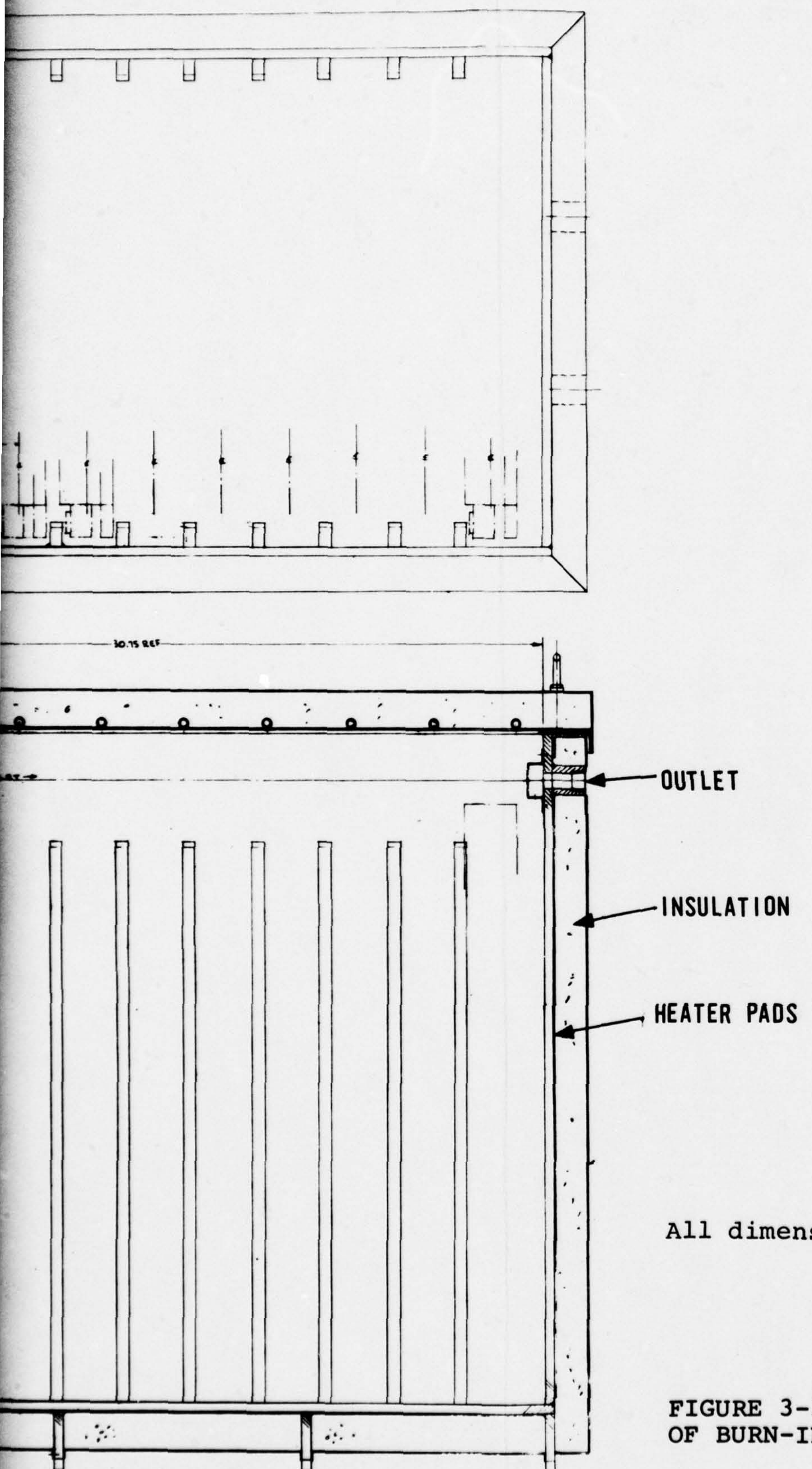
B. INTERCONNECT BOARDS

Figure 3-2 shows the printed wiring board used for interconnecting the chips. The base material is polyimide. It is copper clad on both sides with one ounce material. Where necessary holes are plated through for interfacial connections.

The printed wiring board assembly layout is shown in Figure 3-3. Connectors and pogo pins are mounted on each TAB frame location. Pogo pins make contact with the lead frame so that it may be exercised in a manner determined by an auxiliary printed wiring board plugged into the connector. Printed wiring boards are mounted to the tray shown in Figure 3-4.



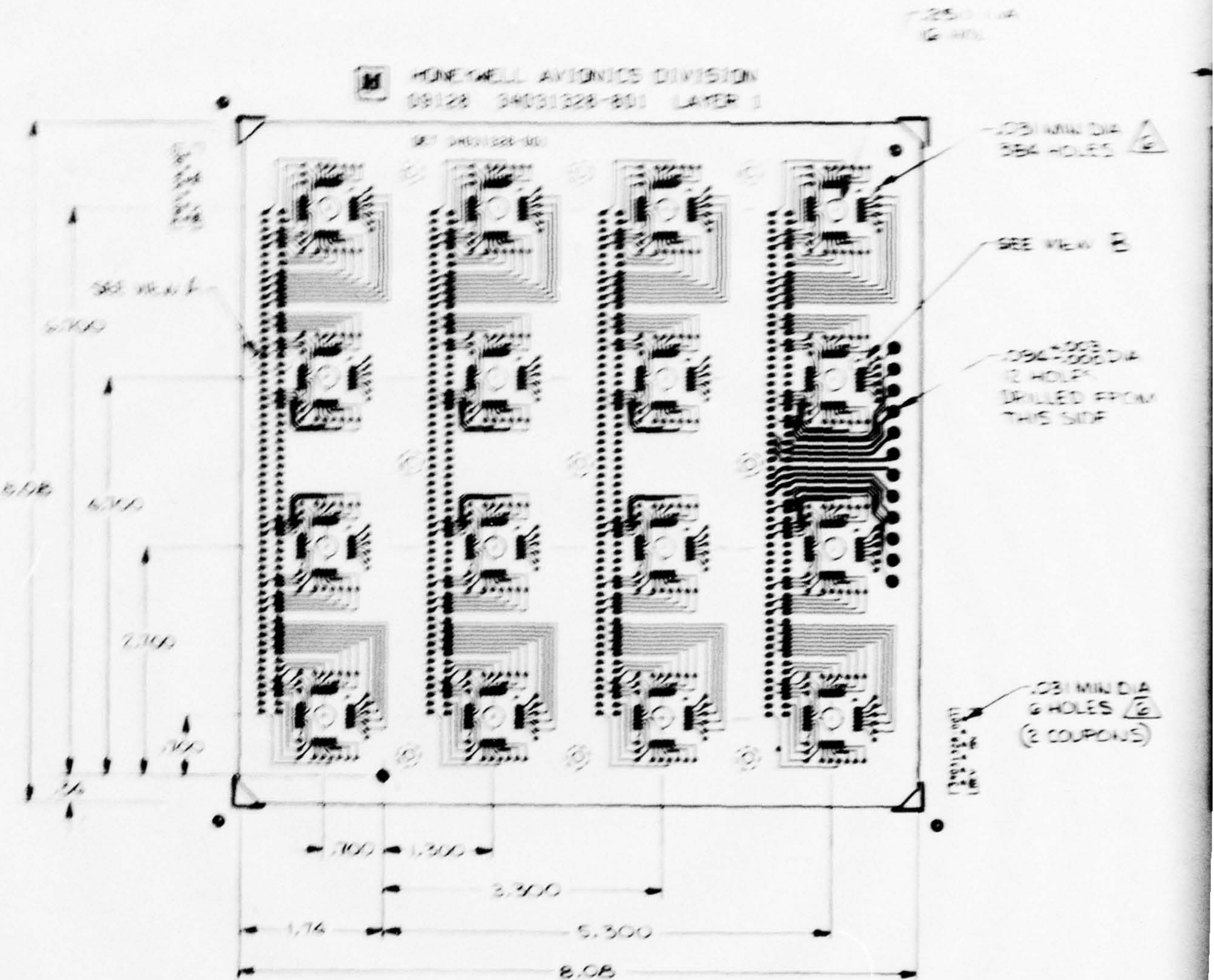
20.5
REF.
30.75 REF
OUTLET
28.0
REF
INLET

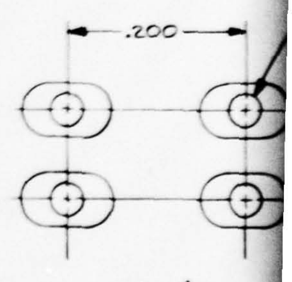


All dimensions in inches.

FIGURE 3-1. LAYOUT DRAWING OF BURN-IN TANK

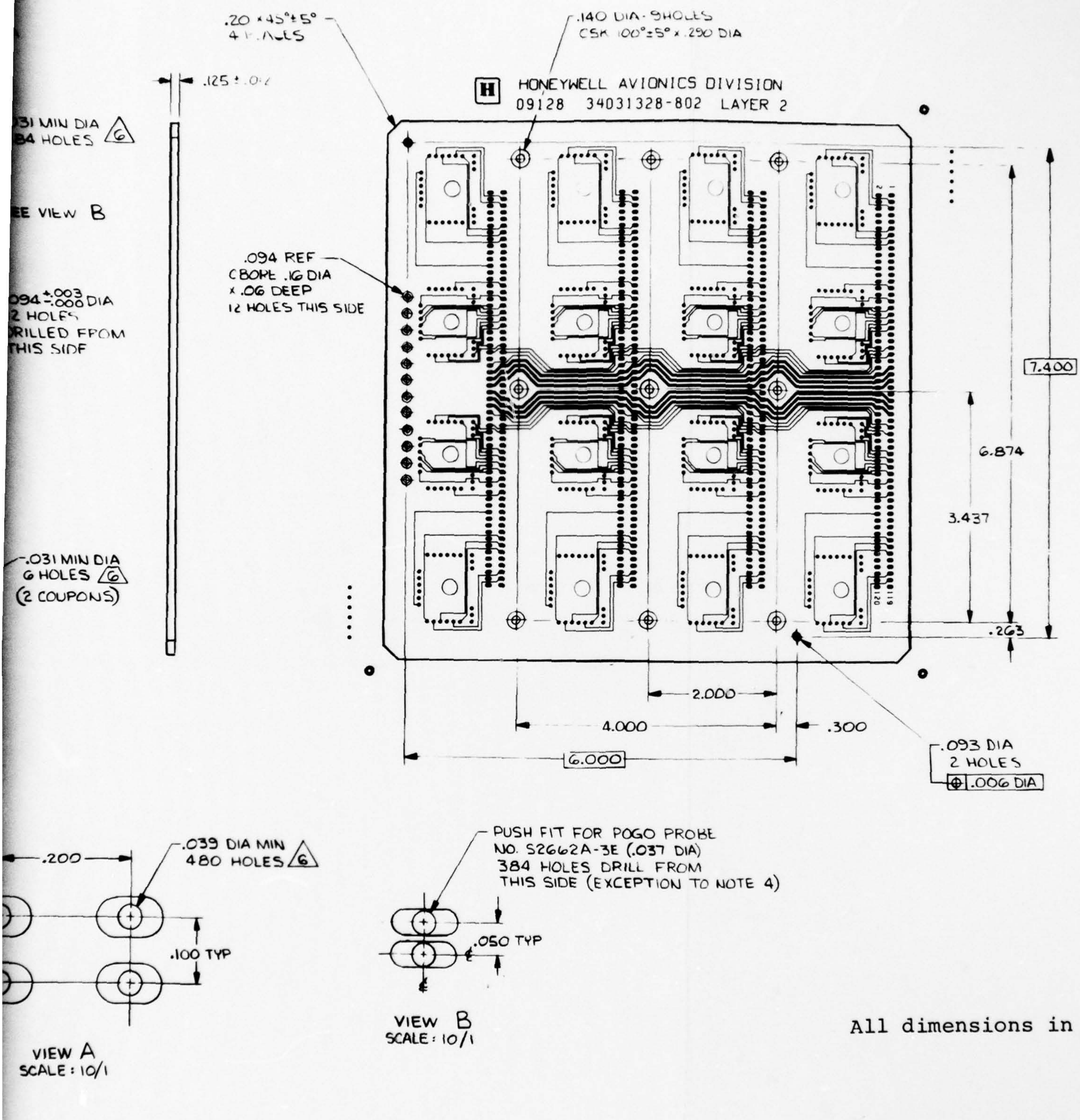
2





VIEW A
SCALE: 10/1

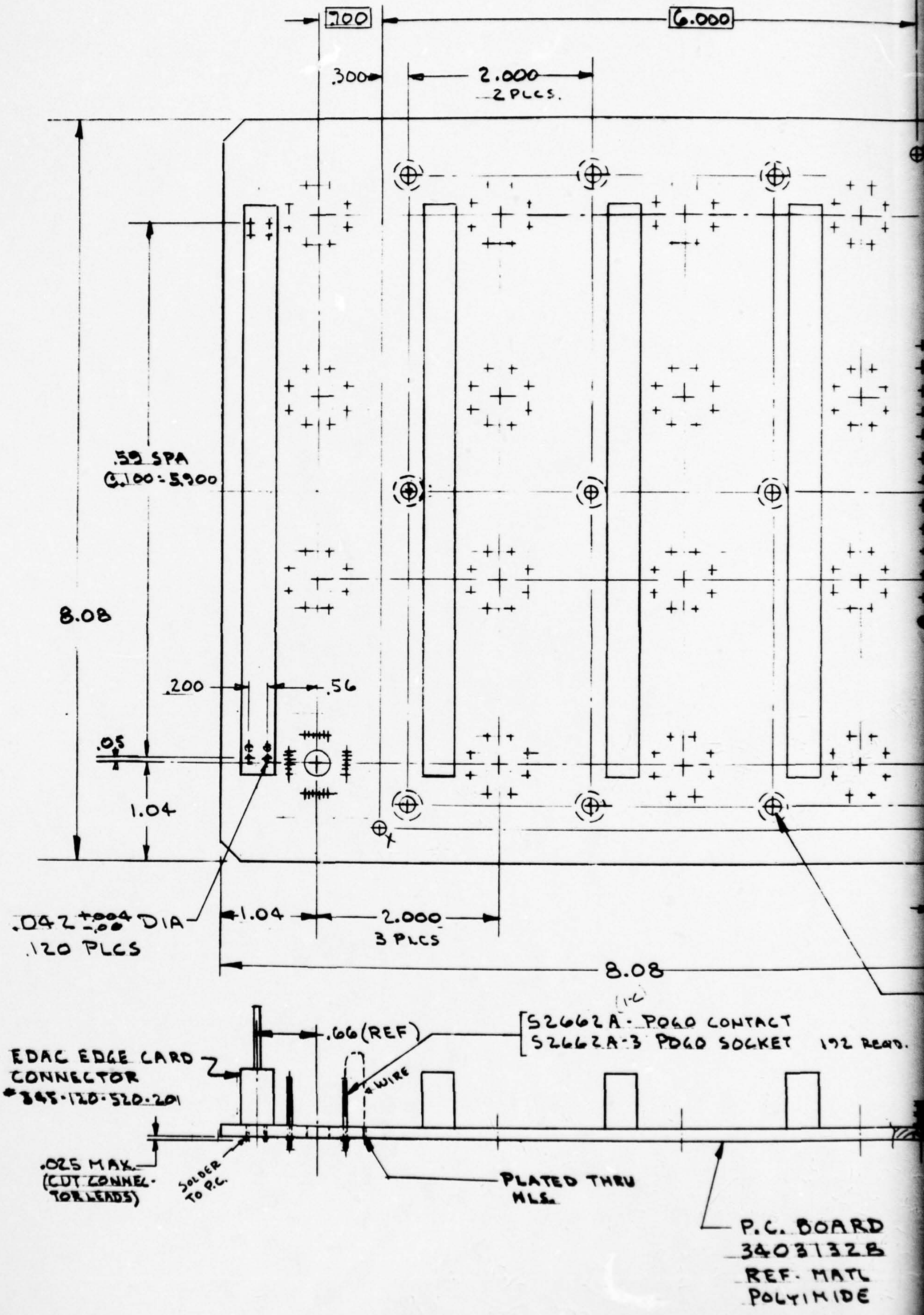
8 - PLOTTER TAPE PT34031328-001 IS THE DOCUMENTATION OF THE ARTWORK MASTER.
7 - THE PRINTED WIRING MANUFACTURER IS RESPONSIBLE FOR THE COMPATIBILITY OF THIS ARTWORK WITH HIS SPECIFIC MANUFACTURING PROCESS AND FACILITES.
6 - PLATED THRU HOLE.
5 - CLEARANCE BETWEEN:
   A. CONDUCTIVE PATHS .008 MIN.
   B. CONDUCTIVE PATHS AND NON-WIRING HOLES .025 MIN.
   C. CONDUCTIVE PATHS AND EDGE OF BOARD .015 MIN.
4 - ANNULAR RING NO BREAKOUT PERMITTED.
3 - CONDUCTOR PATH WIDTH .010 MIN.
2 - NON-LAMINATED PRINTED WIRING BOARD PER ED 21728, TIN-LEAD PLATING-FUSED.
1 - COPPER CLAD POLYIMIDE GLASS LAMINATE, FL-GI-125-C1/1.



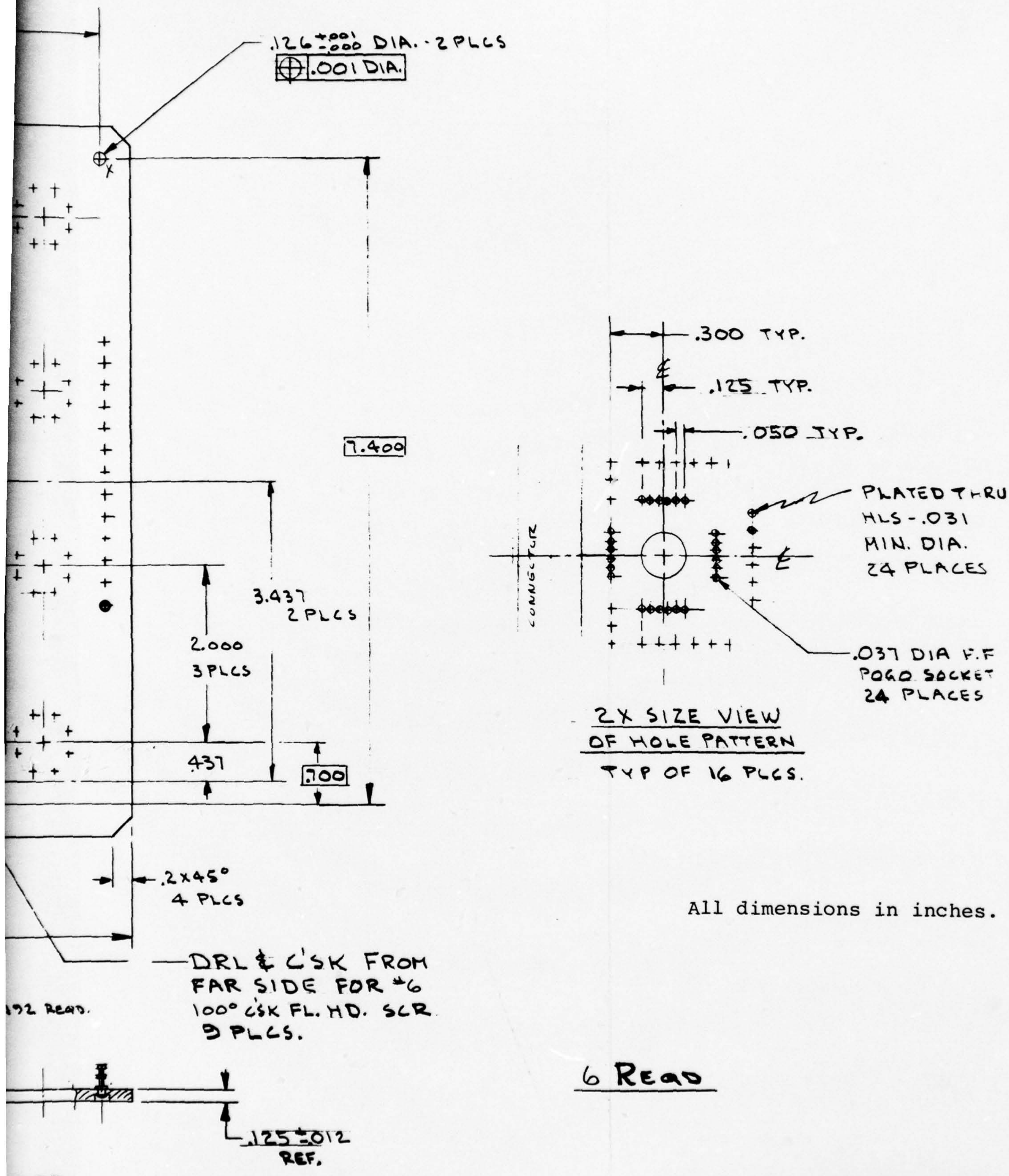
All dimensions in inches.

FIGURE 3-2. PRINTED WIRING BOARD FOR BURN-IN TANK

2

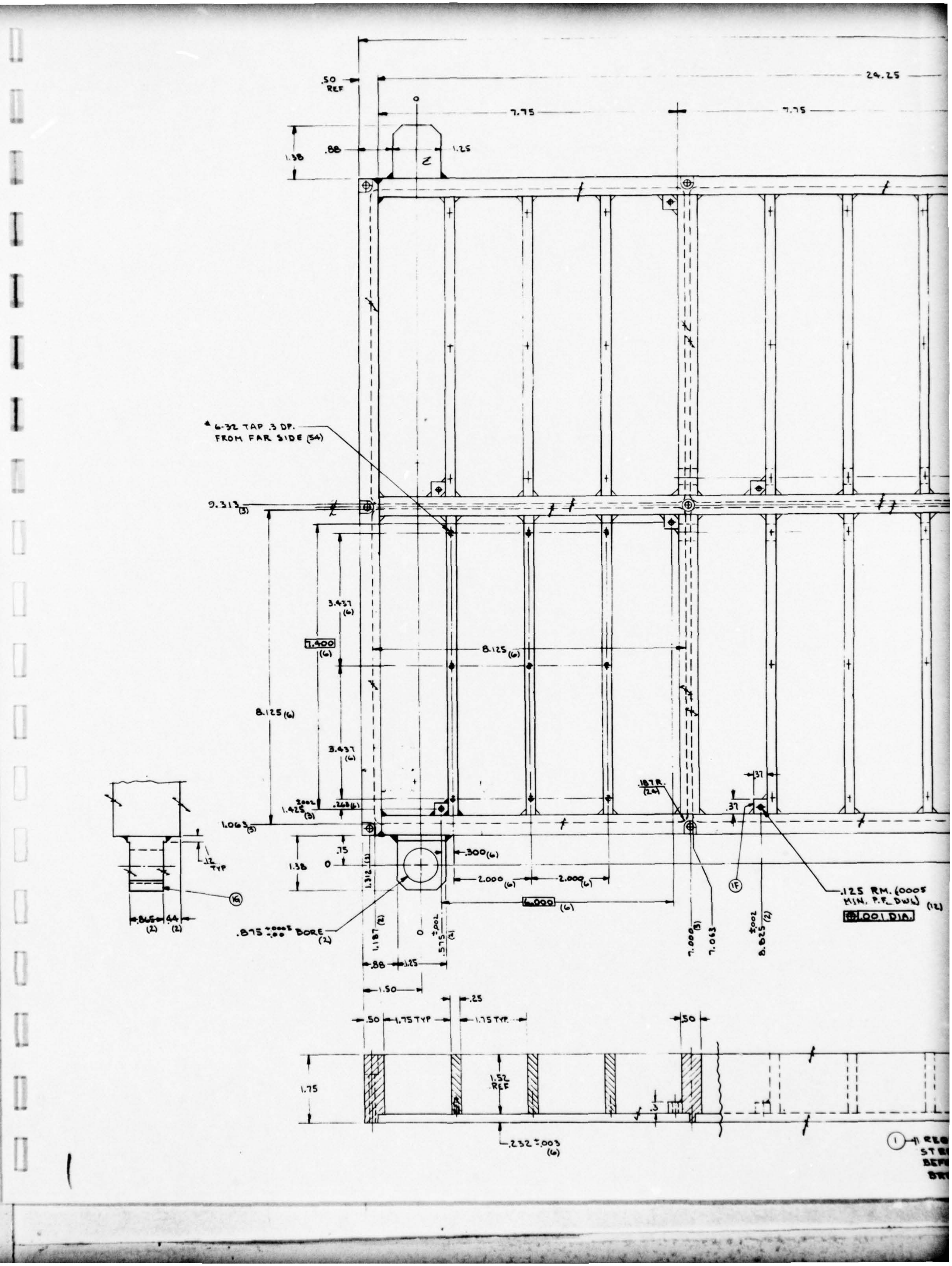


.200
6.000
.300
2.000
2 PLCS.
.59 SPA
@.100 = 5.900
8.08
.200
.56
.05
1.04
.042 +.004 -.00 DIA
.120 PLCS
1.04
2.000
3 PLCS
8.08
S2662A - POGO CONTACT
S2662A-3 POGO SOCKET 192 REQD.
.66(REF)
EDAC EDGE CARD CONNECTOR #345-120-520-201
WIRE
.025 MAX.
(CUT CONNECTOR LEADS)
SOLDER TO P.C.
PLATED THRU HLS.
P.C. BOARD
3403132B
REF. MATL
POLYIMIDE

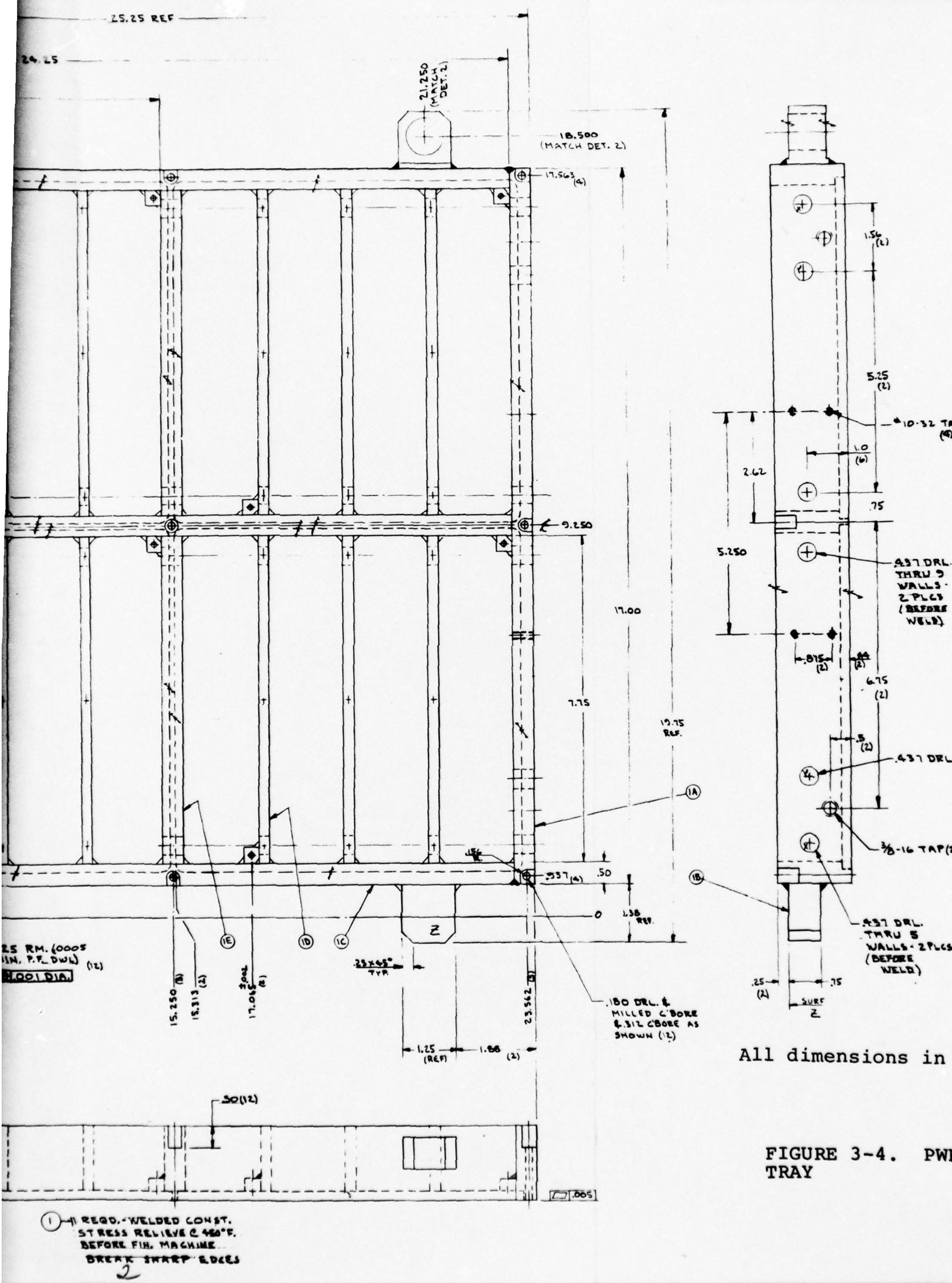


All dimensions in inches.

FIGURE 3-3. PRINTED WIRING BOARD ASSEMBLY



24.25
.50 REF
7.75
7.75
1.38
.88
1.25
* 6-32 TAP .3 DP. FROM FAR SIDE (54)
9.313 (3)
3.437 (6)
7.400 (6)
8.125 (6)
8.125 (6)
3.437 (6)
1.425 (3)
.268 (6)
.187 R. (24)
.37
.37
1.063 (3)
.75
1.38
0
1.312 (3)
.300 (6)
2.000 (6)
2.000 (6)
6.000 (6)
.12 TYP
.865 (2)
.44 (2)
.875 BORE (2)
1.187 (2)
0
.575 (2)
.88
.125
1.50
7.000 (3)
7.063
8.825 (2)
.125 RM. (.0005 MIN. P.F. DWL) (12)
.001 DIA.
.25
.50
1.75 TYP
1.75 TYP.
.50
1.75
1.52 REF
.3
.232 ±.003 (6)



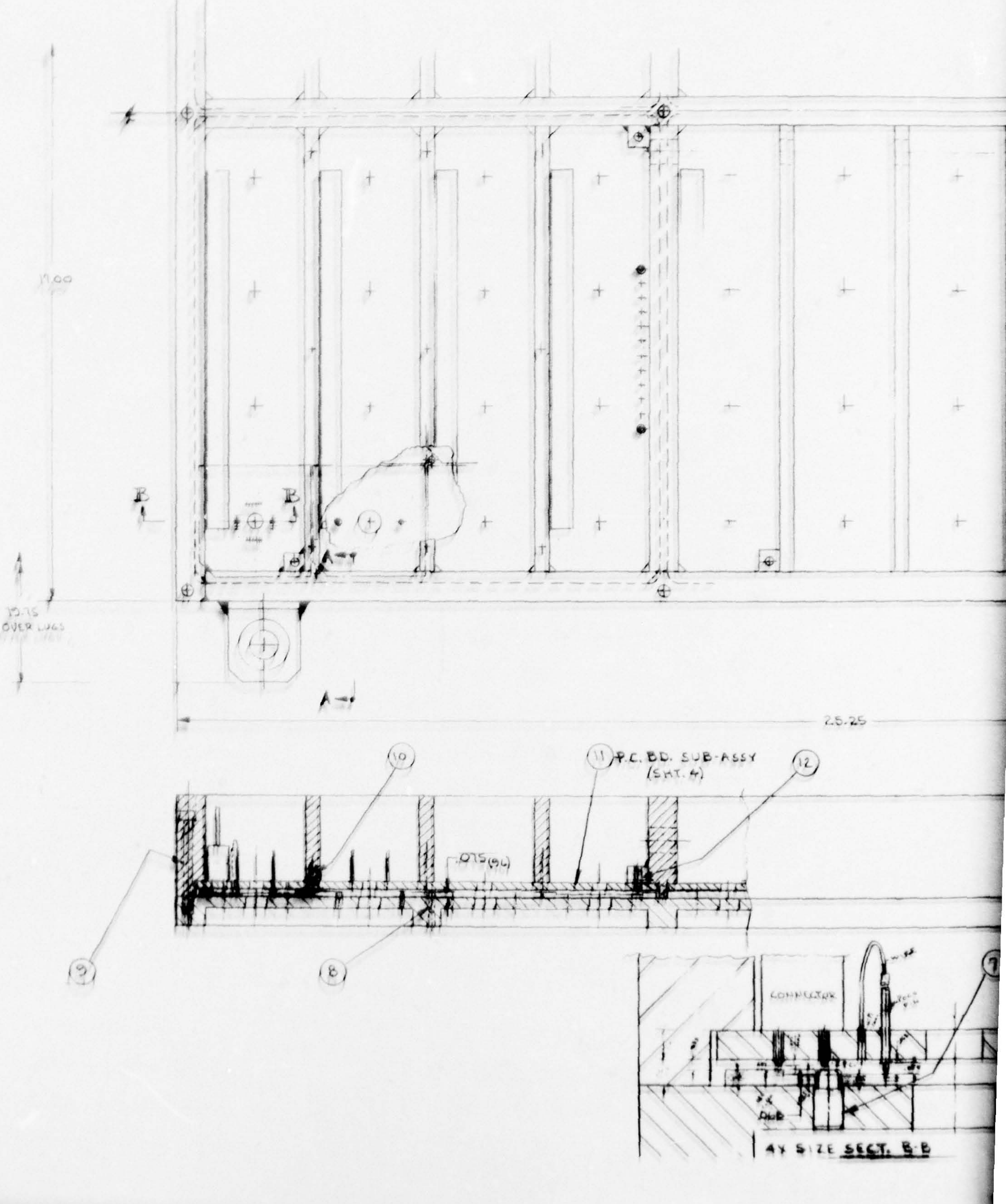
All dimensions in inches.

FIGURE 3-4. PWB MOUNTING TRAY

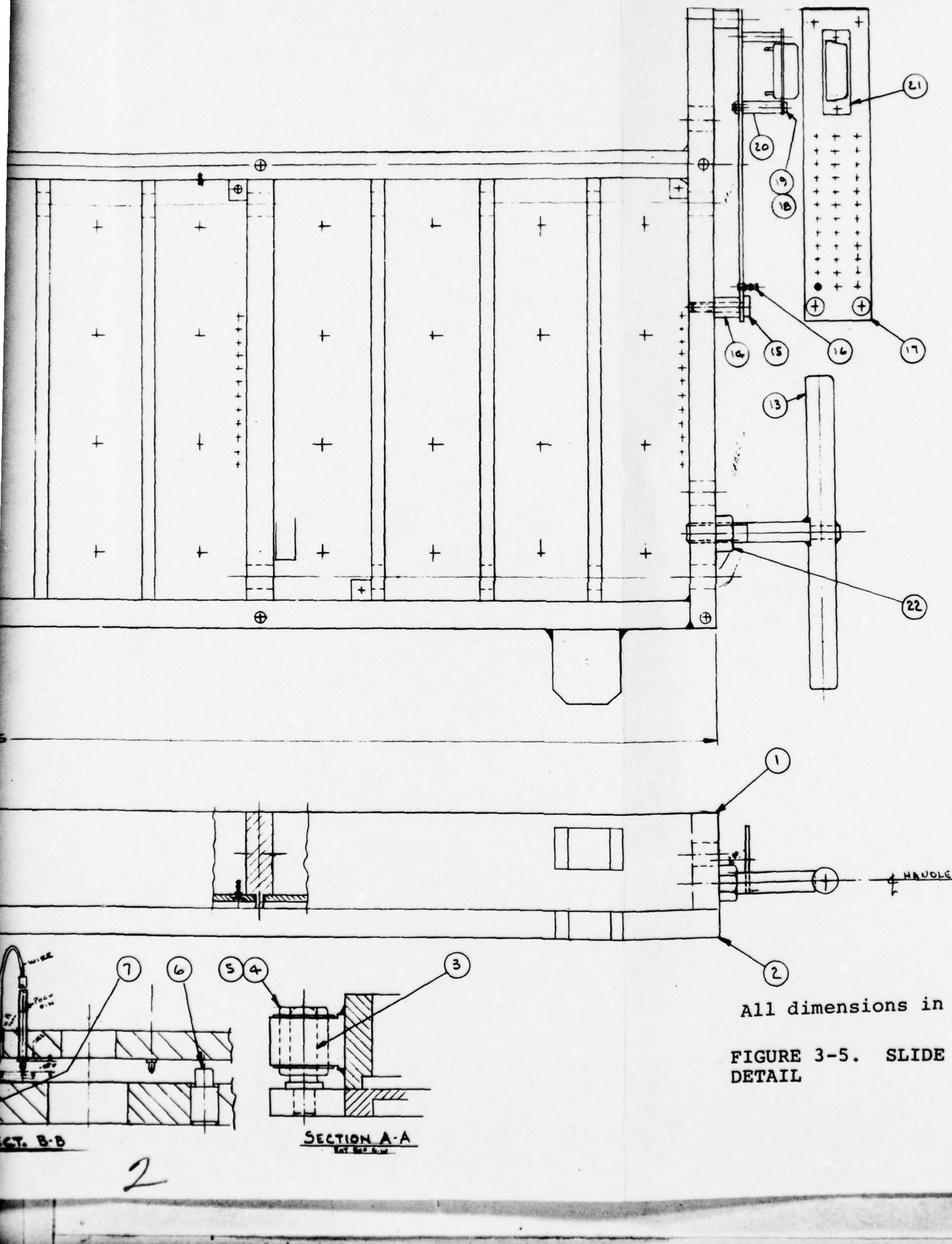
C. SLIDE TRAYS

The tray is made in two parts. One part, which accommodates the printed wiring boards is shown in Figure 3-5. Cabling for interconnection of the twenty-four(24) IC chips is also mounted on this part of the tray. Guides to maintain proper alignment between the two parts of the tray are located in diagonal corners. Registration between the one part mounting the printed wiring boards and the part mounting the TAB devices is most critical and must be maintained in order to make electrical connections to the devices being burned in.

The second part of the tray is detailed in Figure 3-6. This piece mounts the TAB'ed IC chips in proper orientation with respect to the Pogo pins on the printed wiring board. It is bolted to the other part to complete the tray assembly. At each device is a pattern of three pins and a 0.375 inch diameter hole. The two pins on either side of the hole engage the sprocket holes in the 35mm film and maintain alignment for contact with the Pogo pins. To prevent misregistration of the frame, a third pin, installed at 45 degrees from the hole, matches a 45 degree beveled corner on the frame. The function of the hole is to provide fluid flow around the chip and assure proper temperature and heat sinking of the chip.

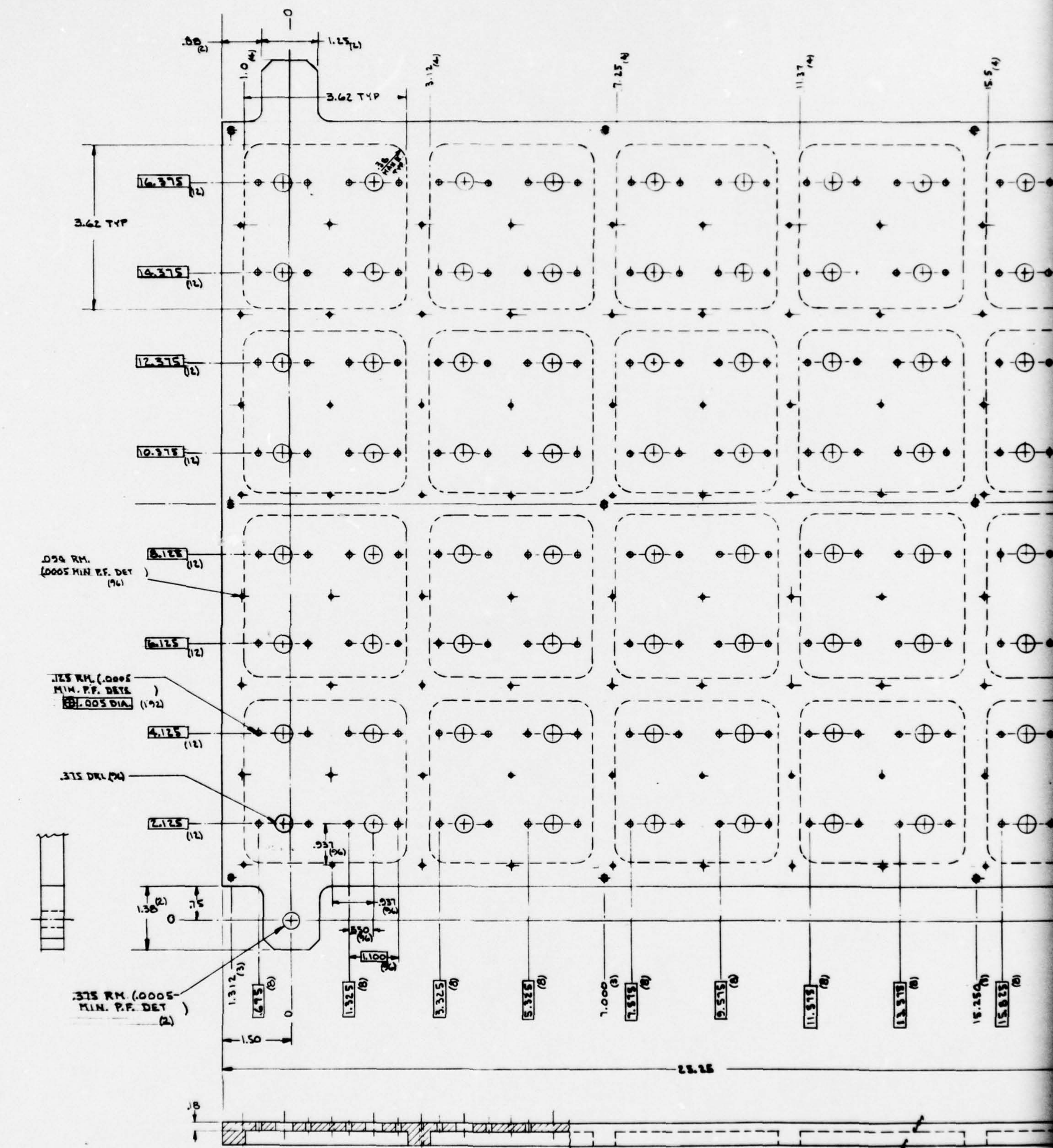


17.00
15.75
OVER LUGS
A
B
B
A
25.25
P.C. BD. SUB-ASSY
(SHT. 4)
10
11
12
.075
9
8
7
CONNECTOR
4X SIZE SECT. B-B



All dimensions in inches.

FIGURE 3-5. SLIDE TRAY DETAIL



(2) 1 REQD - 6061-T651 ALUM
USE 5/8 STK. & STRESS RELIEVE
@ 450° F. ~~BEFORE~~ FIN. MACH.
BREAK SHARP EDGES

All di

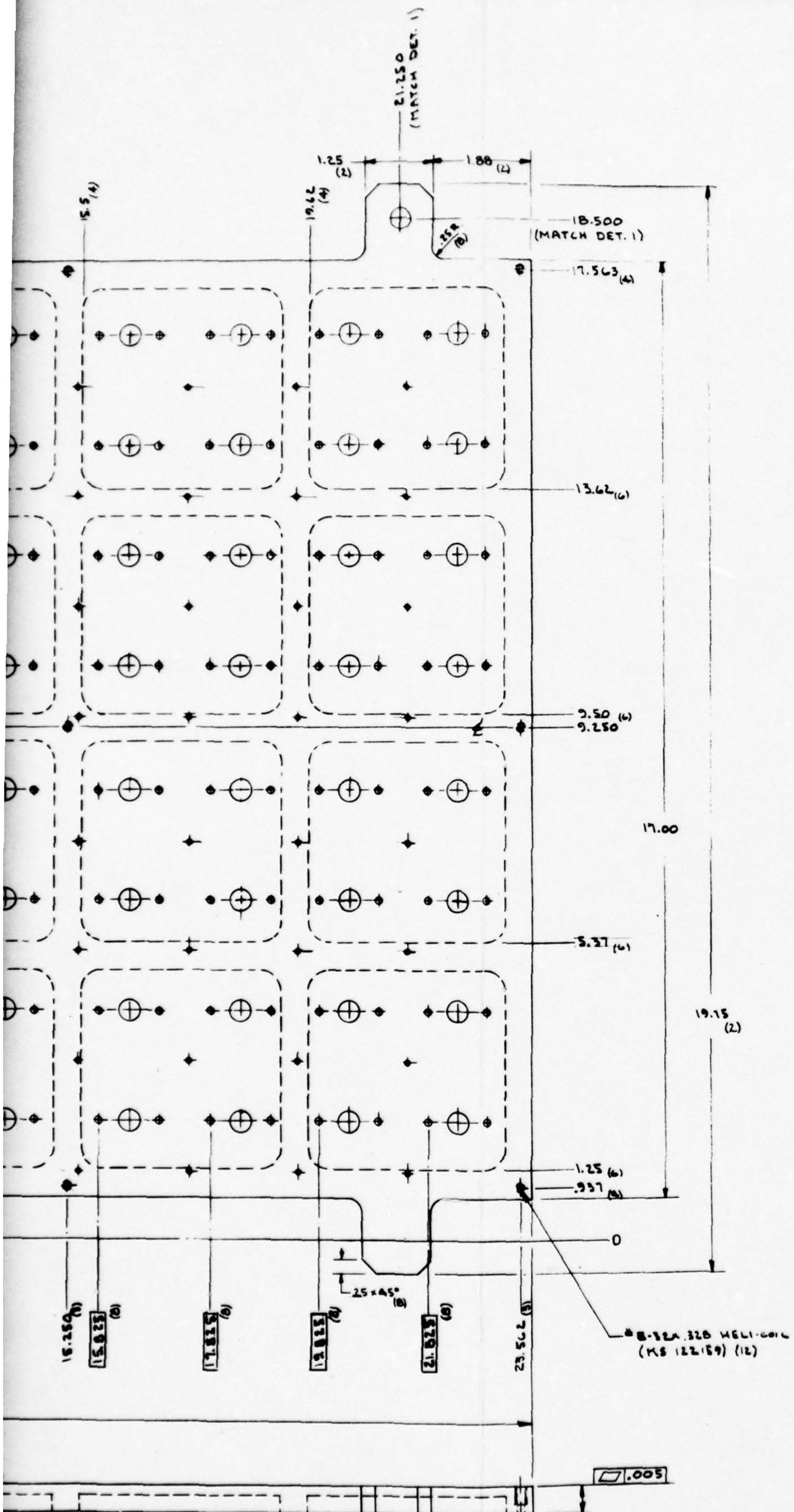


FIGURE 3-6. SLIDE TRAY
DETAIL - CARRIER HOLDER

All dimensions in inches

2

SECTION 4

ENGINEERING SAMPLES

I. FIRST SUBMISSION

A. Electronic Commutator (34030402)

Five electrically and visually acceptable devices were shipped during the previous reporting period.

B. Random Access Memory (34030405)

Five electrically and visually acceptable devices were shipped during the previous reporting period.

C. Minilaser Counter (34030411)

Five electrically and visually acceptable devices were shipped during the previous reporting period.

D. SINCGARS Discriminator (34030408)

The assembly of the Discriminator hybrids was completed and the devices were successfully tested during this reporting period. The Test Report "SINCGARS Discriminator -001" is included in this report as Appendix A. Five electrically and visually acceptable Discriminator hybrids were shipped during this reporting period.

E. Crystal Oscillator (34030417)

1. Thin Film Arrays. Extensive work was performed on the thin film resistor arrays during this reporting period. The sequence of work completed is briefly described below.

The circuit diagram was received from ERADCOM showing the current design as built by Raytheon. This circuit design was analyzed by a Design Engineer from the Producibility and Component Section. General hybrid layout and partitioning was performed by Design Engineering. Requirements for thin film arrays were made based upon space available.

A quotation, requested from Hybrid Systems for the thin film arrays, was submitted and was based on utilizing silicon substrates. These substrate sizes were used in the current hybrid design, when it was decided to build the arrays in-house.

The designs were made using the following guidelines.

A. Substrate material to be silicon or glass (later changed to glazed alumina).
B. Power rating at 40 watts/inch^2.
C. Sheet Resistivity to be 250 ohm/□ max.

D. Line/space geometries of 0.0005/0.0005 inch min.
E. Termination pads to be 0.005 inch in bond area and frozen by design.
F. Resistor values were checked and confirmed by design and frozen.
G. All networks to be passively trimmed only.
H. TCR fixed at not to exceed 100 PPM/°C.

The eight networks were designed and checked by Design Engineering and were found to be acceptable. Figure 4-1 shows the -005 array with one- half mil lines and spaces, Figure 4-2 shows the -006 array. Layouts for resistor networks 34030414-001 through 304030414-004 were sent to Microfab Systems, Palo Alto, California for tooling and 1:1 mask generation. Layouts for 34030414-005 through 34030414-008 were sent to our facility in in Tampa for tooling and 1:1 mask generation. Microfab returned 1:1 mask patterns, and networks 34030414-001 through 004 were photofabricated on glazed ceramic substrates[1]. Preliminary tests showed acceptable resistivities in examples of the first four networks. Some difficulty was encountered in the mask and align phase, due to the fine geometries in these units. Photofabrication of 0.0005/0.0005 inch lines and spaces showed no problem with shorts or opens, but did experience some difficulty in size ratio. Passive trimming done to this date yielded the results shown in Table 4-1.

TABLE 4-1. YIELD AFTER PASSIVE TRIM OF THIN FILM RESISTOR NETWORKS

Device	*Size (mils)*	*Yield Percent*
-001	60 x 60	34
-002	80 x 80	66
-003	80 x 80	70
-004	40 x 40	40
-005	80 x 80	28
-006	80 x 80	37
-007	80 x 80	39
-008	80 x 80	46

2. Breadboard Testing and Trimming Analysis. Breadboard testing of the temperature controller and crystal oscillator circuits have demonstrated that the hybrids can be selected to meet the ±2 ppm frequency over a temperature range of -40°C to +75°C, initially.

---

[1] A change to glazed ceramic was made when it became apparent that silicon and glass would exhibit unacceptable capacitance characteristics.

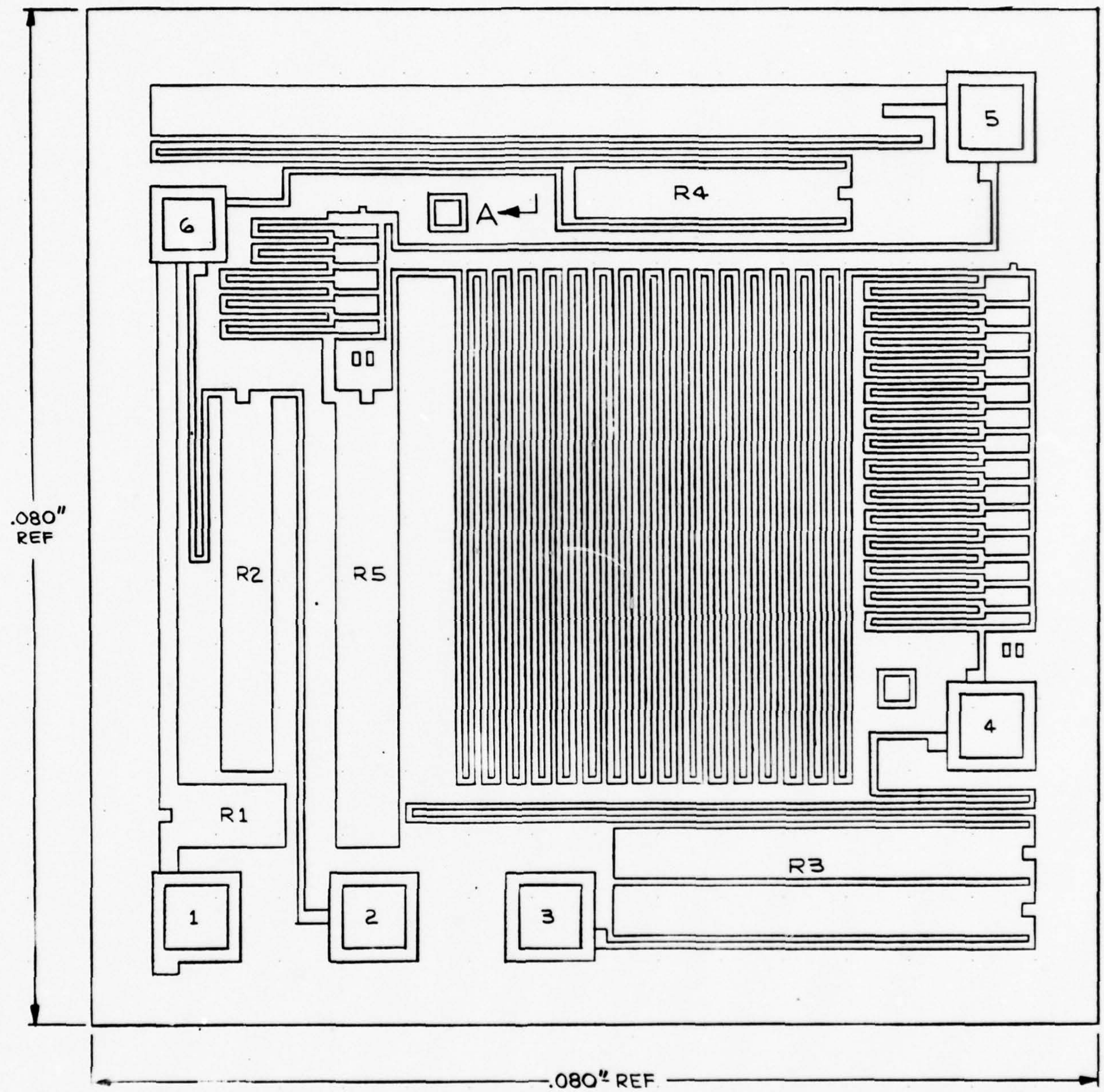


FIGURE 4-1. DASH 5 ARRAY

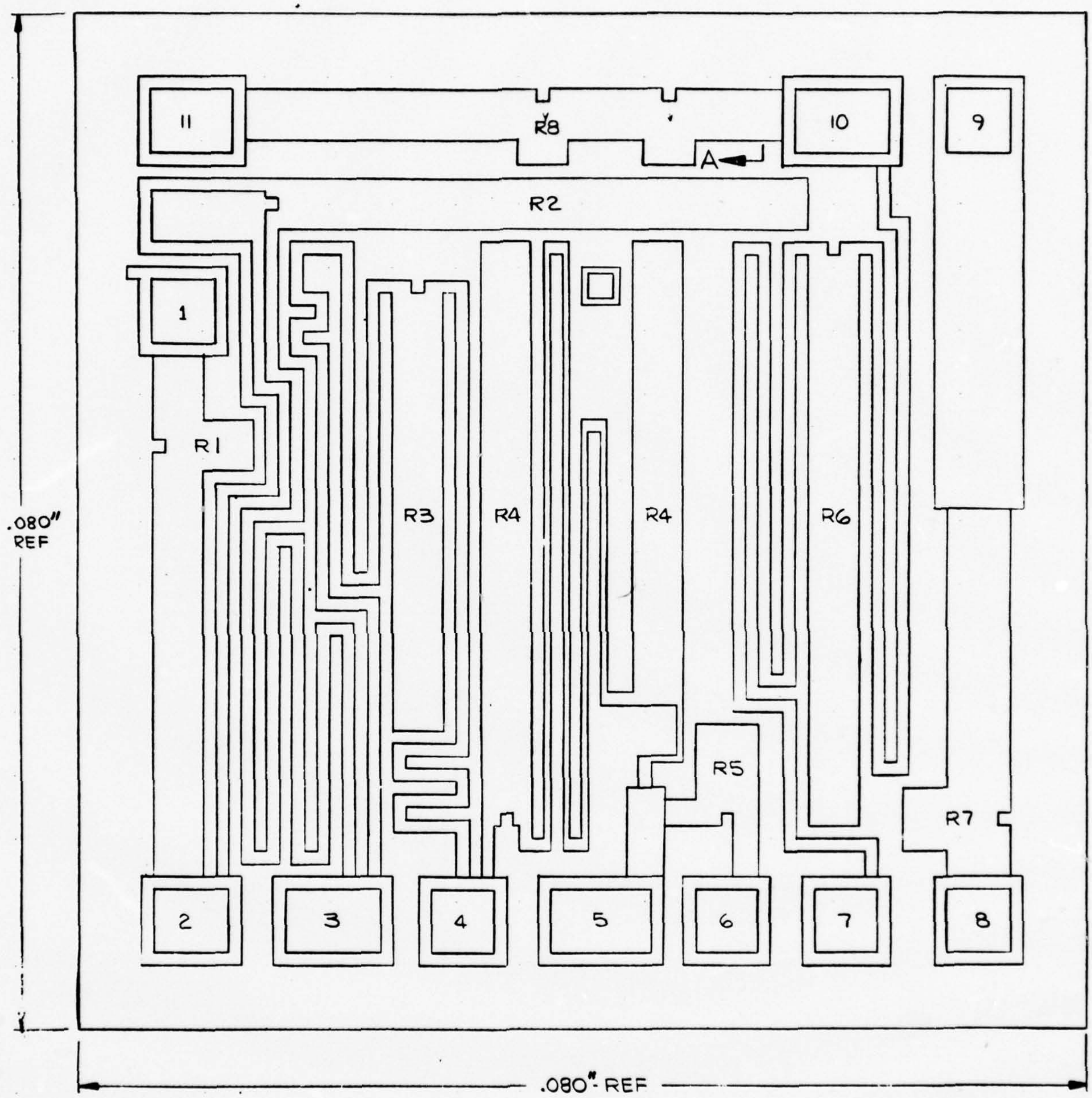


FIGURE 4-2. DASH 6 ARRAY

Initial breadboard tests were also conducted to determine active trim resistor sensitivities (see Table 4-2). The anticipated active trim range and the resistor sensitivity information obtained during breadboard testing could be utilized by the hybrid layout engineer to define the optimum dimensions of the thick film resistors requiring functional trim. This would result in higher functional trim yields and, therefore, a lower unit cost.

Finally breadboard tests were conducted to determine the possibility of making the required compensating curve adjustment by inserting the crystal into the circuit and operating the oscillator at the upper and/or lower turning point to select the proper values of R47 and R48 (see Tables 4-3, 4-4, and 4-5). All three crystals tested in the breadboard would fail to meet the ±2 ppm requirement from center frequency when R47 and R48 are trimmed to the values indicated by Piezo's frequency/temperature curves, using the current trim procedure. But by utilizing this new technique, crystal S/N 54 (R47 = 10K ohm, R48 = 17K ohm) and crystal S/N 64 (R47 - 10K ohm, R48 - 25K ohm) would meet the ±2 ppm requirement from center frequency over the temperature range of -40°C to +75°C, while S/N 12 would display marginal response with R47 = 10K ohm and R48 - 24K ohm. Initial data indicates that the new approach will result in the minimum frequency change from center frequency over the temperature range of -40°C to +75°C. This will contribute to improved frequency stability versus temperature resulting in higher trim yields and lower unit cost.

3. Assembly. The Engineering Samples are now in the process of being assembled. Figure 4-3 shows a photograph of the Crystal Oscillator after component attach, including the thin film arrays, but before wire bonding. Note that the device is printed "two-up" on a 2 x 2 inch substrate. The open space in the upper right hand corner is allocated for the crystal. The passive trim mark in the thick film resistors are clearly visible. The trim mark in the thin film arrays are too fine to be detectable on this photograph. Note also that the substrate has been pre-scored so that it can be easily broken after assembly. Figure 4-5 shows the current schedule. The first five Engineering Samples were to be shipped at the end of April.

F. Temperature Controller (34030415)

The work done on the resistor arrays for the Crystal Oscillator applies to the Temperature Controller as well as similar arrays used for this hybrid. During this reporting period the Temperature Controller hybrids were assembled and submitted to active trim. Figure 4-4 shows a photograph of the assembled device after wire bonding. The wires are barely visible on the picture. As with the Crystal Oscillator the passive trim cuts can be easily distinguished.

The schedule shown on Figure 4-5 applies to the Temperature Controller as well. Engineering samples were delivered at the end of April.

TABLE 4-2. FUNCTIONAL TRIM RESISTOR SENSITIVITIES

Resistor Designation	Circuit	ΔR (Ohm)	ΔV (mV)	ΔF (Hz)
R72	Crystal	100	1	
	Osc	1,000	12	
R71	Crystal	100	1	
	Osc	1,000	12	
R98	Crystal	2 to 3	1	
	Osc	10	2 to 3	
		100	23	
R97	Crystal	10	1	
	Osc	100	9	
R70	Crystal	100	1	
	Osc	1,000	8	
R69	Crystal	100	1 to 2	
	Osc	1,000	15	
R63	Crystal	200	1	
	Osc	1,000	6	
		3,000	16	
R64	Crystal	100	0.5 to 1	
	Osc	1,000	6 to 8	
R76	Crystal	100	1 to 2	
	Osc	1,000	15	
R104	Crystal	1,000	1	
	Osc	10,000	10	
R78	Crystal	1,000		1
	Osc	10,000		11 to 16
R75	Crystal	100	2 to 3	
	Osc	1,000	15	
		10,000	135	
R83	Crystal	500		1 to 2
	Osc	1,000		4
		10,000		38
R80	Crystal	100		1
	Osc	1,000		11
		10,000		100

TABLE 4-2. FUNCTIONAL TRIM RESISTOR SENSITIVITIES (Continued)

Resistor Designation	Circuit	ΔR (Ohm)	ΔV (mV)	ΔF (Hz)
R6	Temp	1,000	1	
	Cont	10,000	9	
R2	Temp	200	1	
	Cont	1,000	5	
		10,000	50	
R5	Temp	10	3	
	Cont	100	32	
		1,000	324	
R3	Temp	10	1	
	Cont	100	7 to 8	
		1,000	70	
R56	Temp	20	1	
	Cont	100	6	
		1,000	55	
R57	Temp	10	0.5 to 1	
	Cont	100	7	
		1,000	67	

TABLE 4-3. FREQUENCY/TEMPERATURE STABILITY OF CRYSTAL S/N 54

Temp. (^{o}C)	Frequency (R48 10K)	(R48 12K)	(R48 15K)	(R48 17K)	(R48 20K)
-40	7403	7425	7453	7469	7490
-30	7428	7446	7470	7483	7501
-20	7429	7443	7463	7474	7489
-10	7436	7447	7463	7472	7483
0	7468	7476	7486	7481	7488
10	7490	7494	7499	7489	7494
20	7496	7497	7499	7492	7495
23	7499	7499	7499	7497	7497
30	7494	7490	7486	7484	7482
40	7497	7490	7482	7477	7470
50	7507	7497	7485	7477	7468
55	7511	7500	7484	7476	7463
60	7512	7498	7479	7470	7456
70	7523	7505	7481	7467	7449
75	7543	7522	7496	7480	7460

NOTES:

1. All frequencies are 21, 93X, XXX Hz, where the X, XXX values are listed in the frequency column for each temperature/R48 combination.

2. The value of R47 was 10K ohms.

3. The value of the 25K pot was 16, 170 ohms.

4. The trim values were calculated to be R47 = 10K and R48 = 14K using current trim method; (UTP-LTP) F_X/F_S.

TABLE 4-4. FREQUENCY/TEMPERATURE STABILITY OF CRYSTAL S/N 12

Temp. (^{o}C)	Frequency (R48 10K)	(R48 12K)	(R48 14K)	(R48 16K)	(R48 18K)	(R48 20K)	(R48 22K)	(R48 24K)
-40	7352	7374	7393	7410	7424	7435	7450	7460
-30	7393	7410	7426	7441	7453	7465	7475	7484
-20	7396	7412	7426	7439	7450	7459	7468	7476
-10	7411	7423	7433	7443	7451	7459	7465	7472
0	7437	7446	7454	7461	7467	7472	7478	7482
10	7468	7473	7478	7482	7485	7488	7491	7494
20	7488	7488	7490	7491	7492	7492	7493	7493
30	7495	7492	7490	7487	7485	7483	7481	7480
40	7505	7499	7493	7488	7483	7479	7475	7471
50	7523	7513	7505	7497	7490	7484	7478	7473
55	7530	7519	7508	7499	7490	7482	7475	7469
60	7534	7521	7509	7498	7488	7479	7471	7464
70	7553	7534	7518	7504	7490	7478	7467	7457
75	7578	7557	7538	7521	7506	7493	7480	7469

NOTES:

1. All frequencies are 21,93X,XXX Hz, where the X,XXX values are listed in the frequency column for each temperature/R48 combination.

2. The value of R47 was 10K ohms.

3. The value of the 25K pot was 17,330 ohms.

4. The trim values were calculated to be R47 = 10K and R48 = 20K using current trim method; (UTP-LTP) F_X/F_S.

TABLE 4-5. FREQUENCY/TEMPERATURE STABILITY OF CRYSTAL S/N 64

Temp	Frequency							
Temp (°C)	(R48 23K)	(R48 26K)	(R48 28K)	(R48 29K)	(R48 30K)	(R48 31K)	(R48 32K)	(R48 34K)
-40	7459	7475	7484	7487	7491	7494	7497	7504
-30	7477	7490	7498	7502	7505	7508	7512	7518
-20	7478	7489	7495	7497	7500	7502	7504	7510
-10	7472	7481	7486	7488	7490	7493	7494	7499
0	7483	7489	7493	7495	7496	7498	7500	7503
10	7494	7498	7501	7502	7503	7504	7505	7507
20	7491	7493	7494	7494	7495	7496	7497	7497
30	7499	7497	7495	7495	7494	7494	7494	7493
40	7487	7483	7480	7479	7478	7476	7475	7473
50	7488	7480	7476	7474	7472	7470	7468	7464
55	7487	7478	7473	7471	7468	7466	7464	7460
60	7480	7470	7464	7461	7458	7456	7453	7449
70	7472	7460	7452	7448	7445	7442	7438	7431
75	7486	7471	7462	7458	7454	7450	7446	7438

NOTES:

1. All frequencies are 21,93X,XXX Hz, where the X,XXX values are listed in the frequency column for each temperature/R48 combination.

2. The value of R47 was 10K ohms.

3. The value of the 25K pot was 18,200 ohms.

4. The trim values were calculated to be R47=10K and R48 = 23K using the current trim method; (UTP-LTP) F_X/F_S.

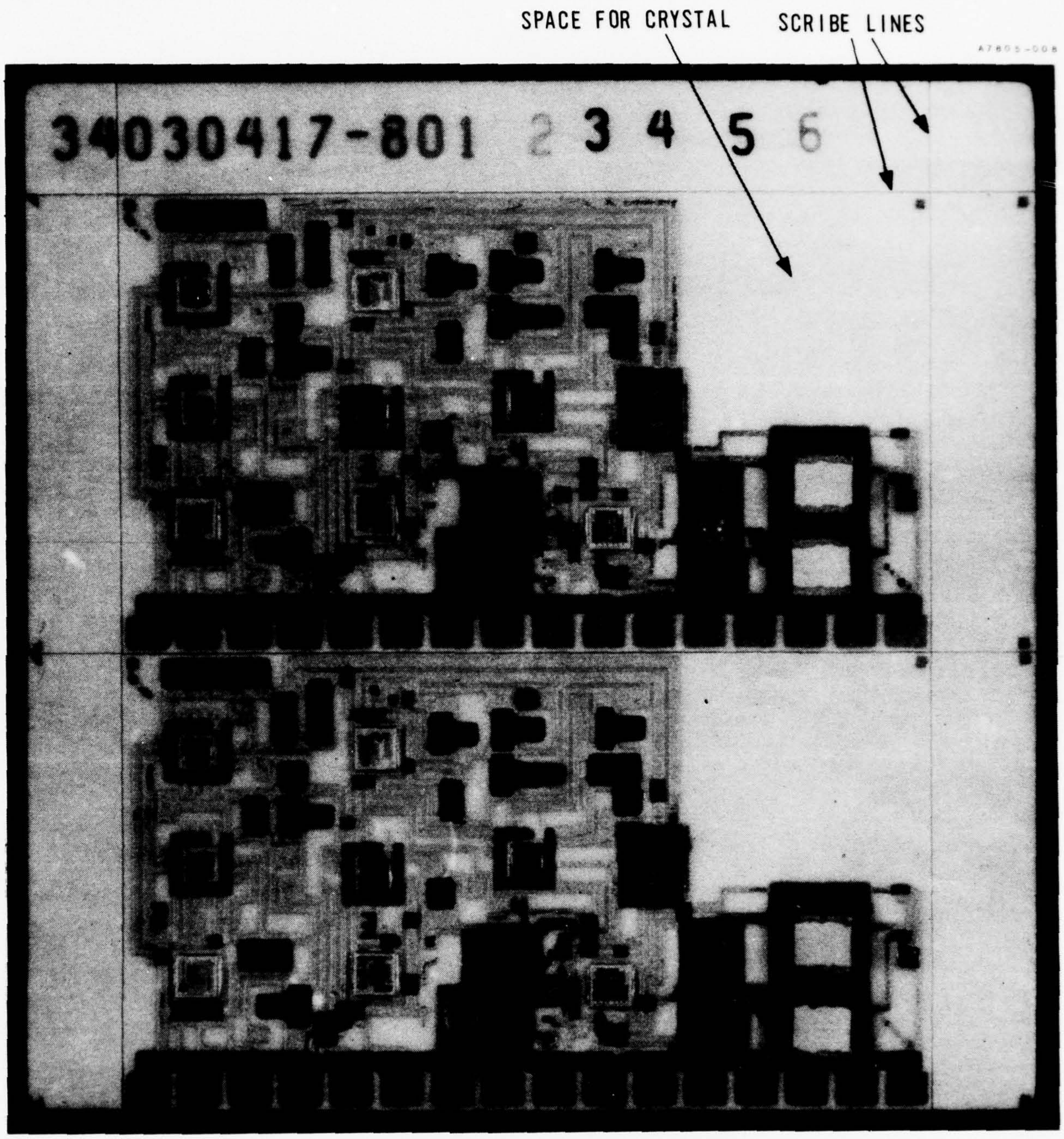


FIGURE 4-3. CRYSTAL OSCILLATOR
(PRIOR TO CRYSTAL MOUNT)

A7805-007

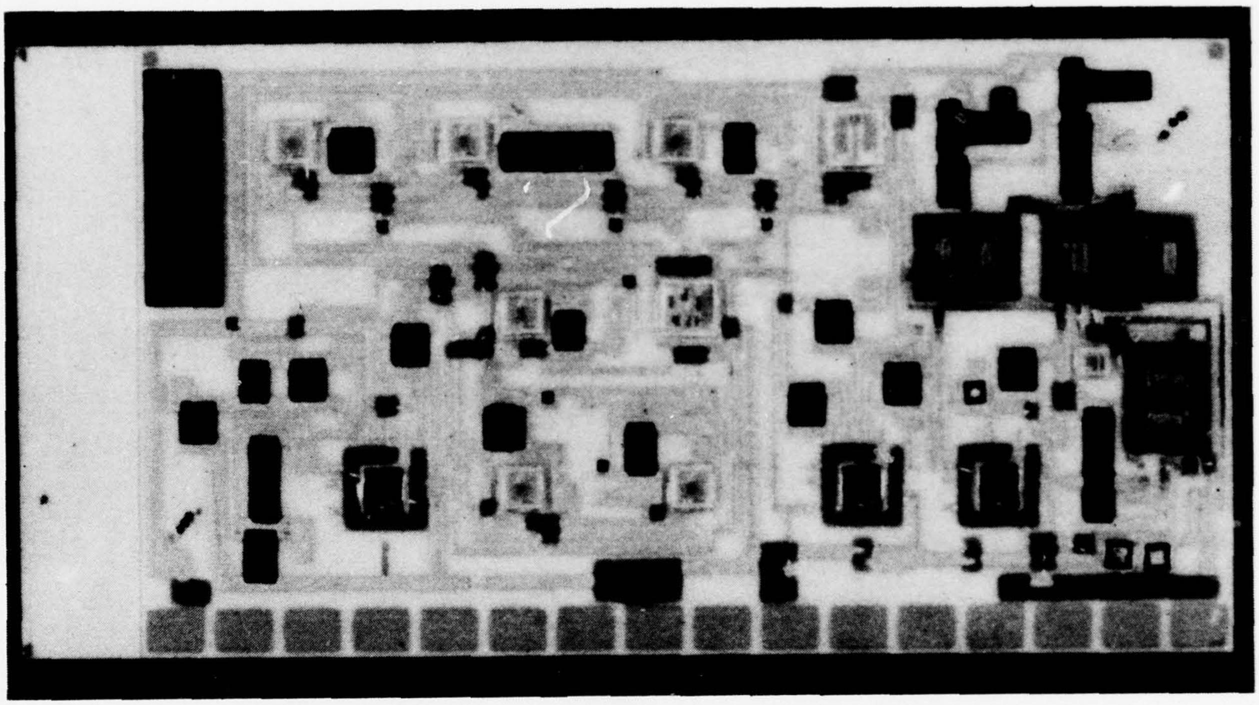


FIGURE 4-4. TEMPERATURE CONTROLLER

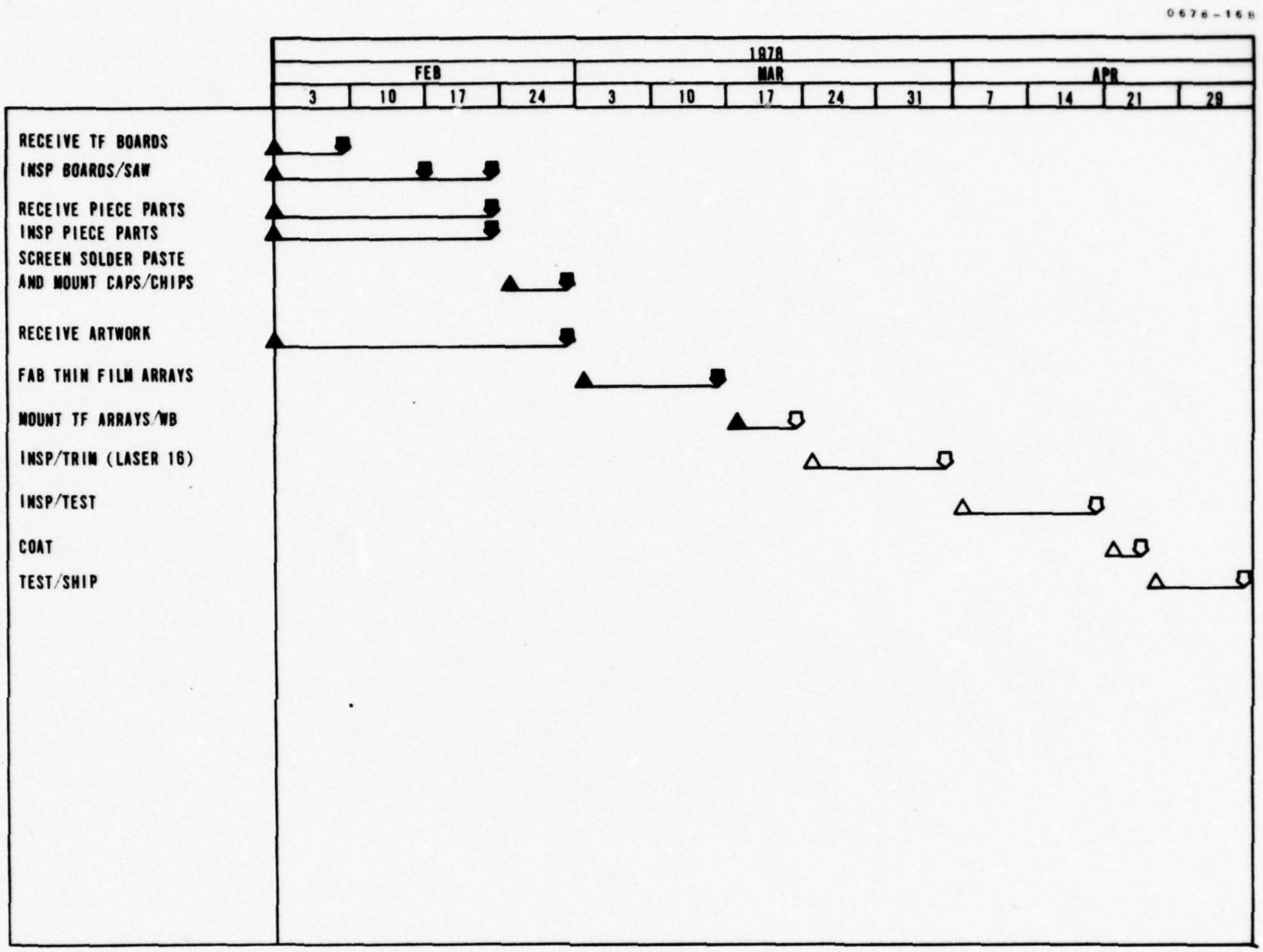


FIGURE 4-5. MANUFACTURING SCHEDULE - FIRST SUBMISSION - TEMPERATURE CONTROLLER/CRYSTAL OSCILLATOR

II SECOND SUBMISSION

After thorough technical discussions with the ECOM Program Director it has been decided to delete the Third Submission Engineering Samples for reasons of cost effectiveness and schedule. Because of this the Second Submission Samples will be completely TAB bonded whenever possible. The schedule due date for this submission will be 30 June 1978, the same date as originally planned for the Third Submission.

At the same time it was decided not to continue beyond the First Engineering Samples for the Crystal Oscillator and Temperature Controller devices because of their great complexity and extensive manual active test and trim.

A. Electronic Commutator (34030402)

The substrates for the Electronic Commutator second submission samples have been fabricated and are in stock. Wafer preparation prior to bumping has begun with laser enhancement of the reject marks and metallization of the barrier layers. These tasks have seen some delay because the delivery of the wafers was later than promised by the vendor. The schedule for manufacturing of the second samples is shown in Figure 4-6.

B. Random Access Memory (34030405)

The substrates for the RAM second submission samples have been fabricated and are in stock. *Delivery of the wafers has been slipped to* early in the next reporting period. Figure 4-7 shows the schedule for manufacturing of the second set of engineering samples.

C. Minilaser Counter (34030411)

The substrates for the Minilaser Counter samples have been fabricated and are in stock. Most of the wafers have experienced delays in delivery and are not expected in until early May. Figure 4-8 shows the schedule for manufacturing of the second submission samples of the Minilaser Counter.

D. SINCGARS Discriminator (34030408)

The substrates for the Discriminator Hybrid have been fabricated and are in stock. One of the wafer types has been received and is being metallized in preparation for bumping. The second wafer is not due until the middle of the next reporting period. Bump masks, tape and tooling have been received and are in stock. Figure 4-9 shows the manufacturing schedule for the SINCGARS Discriminator second engineering samples.

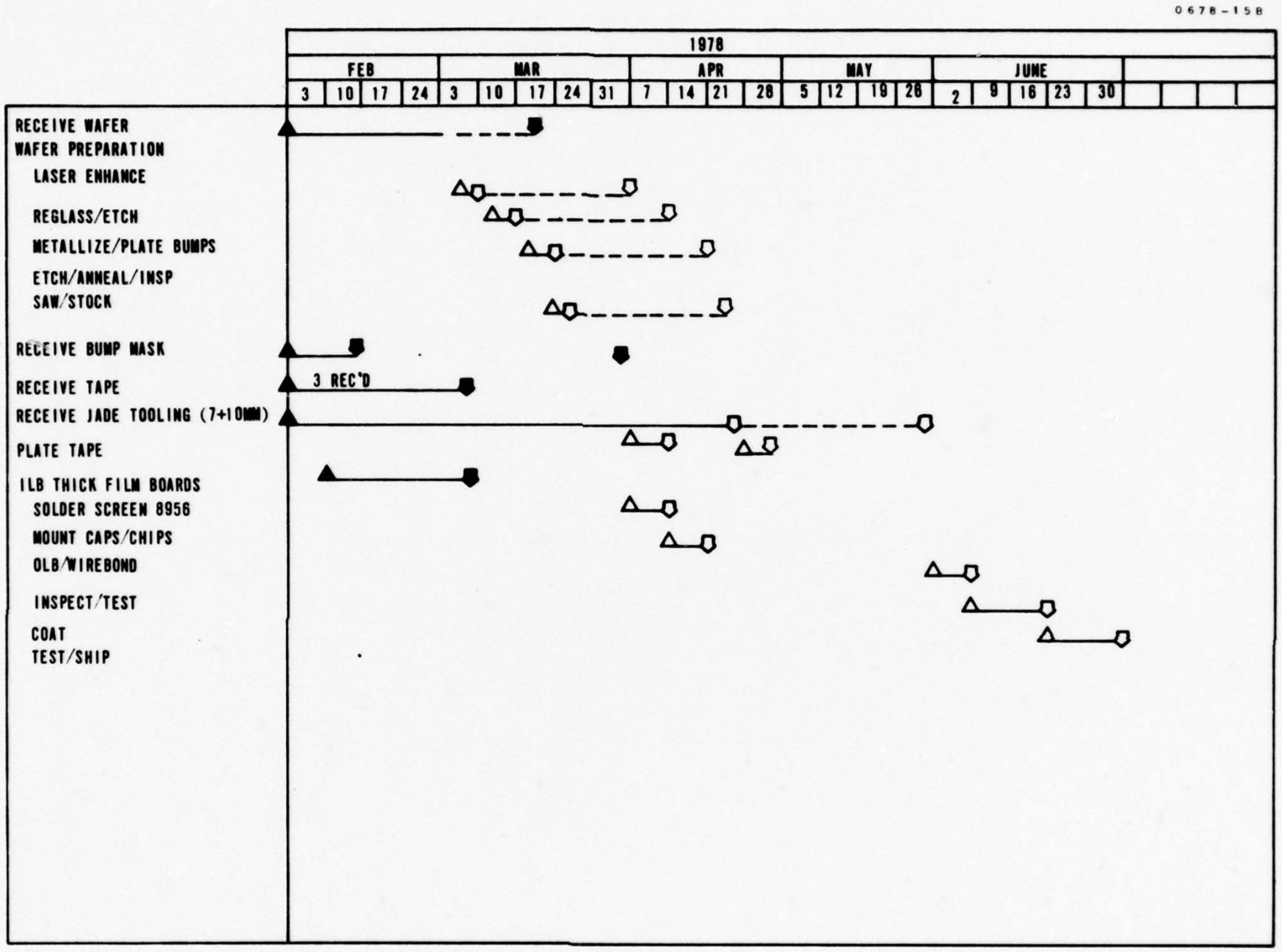


FIGURE 4-6. MANUFACTURING SCHEDULE - SECOND SUBMISSION - ELECTRONIC COMMUTATOR

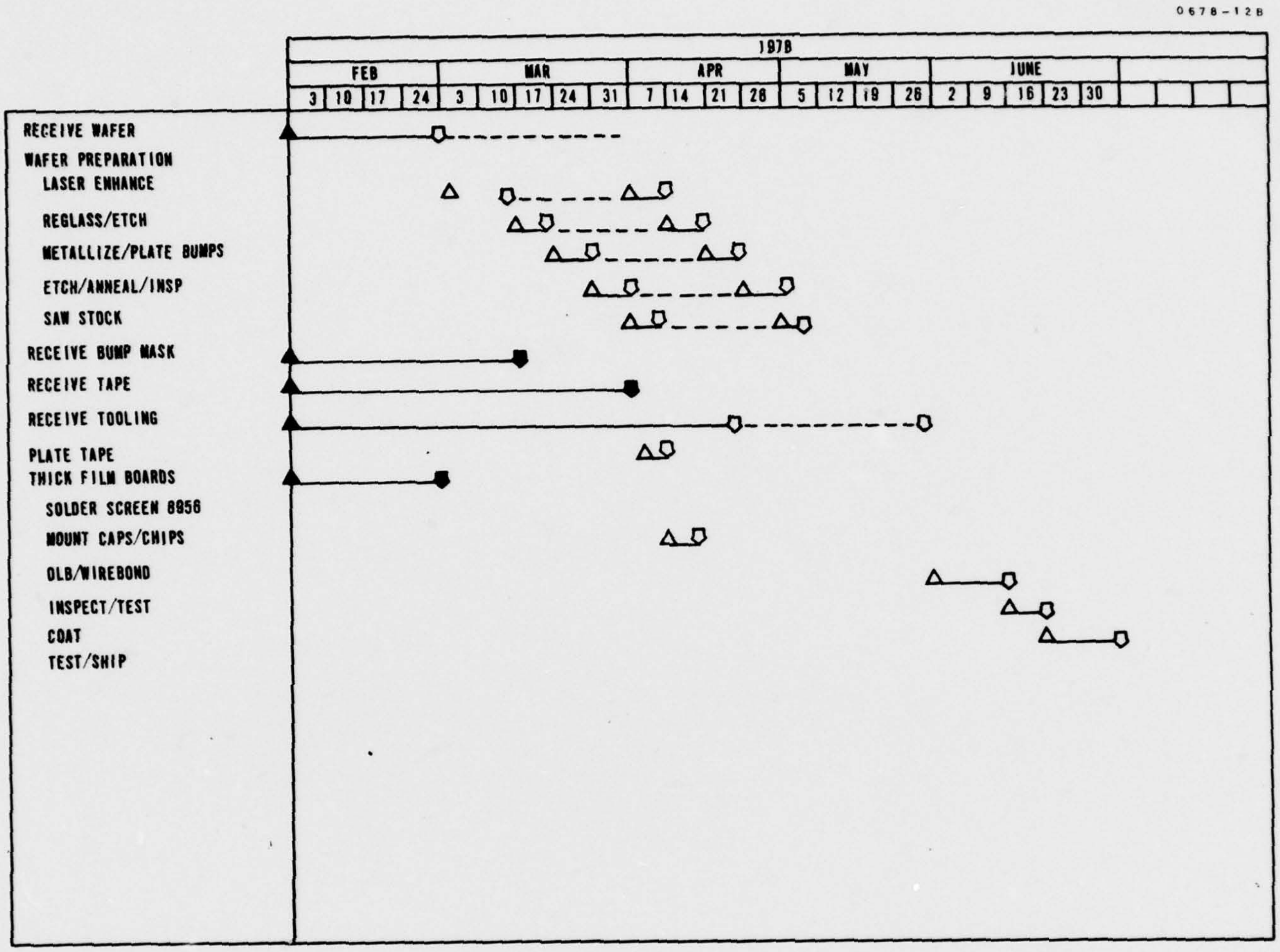


FIGURE 4-7. MANUFACTURING SCHEDULE - SECOND SUBMISSION - RAM

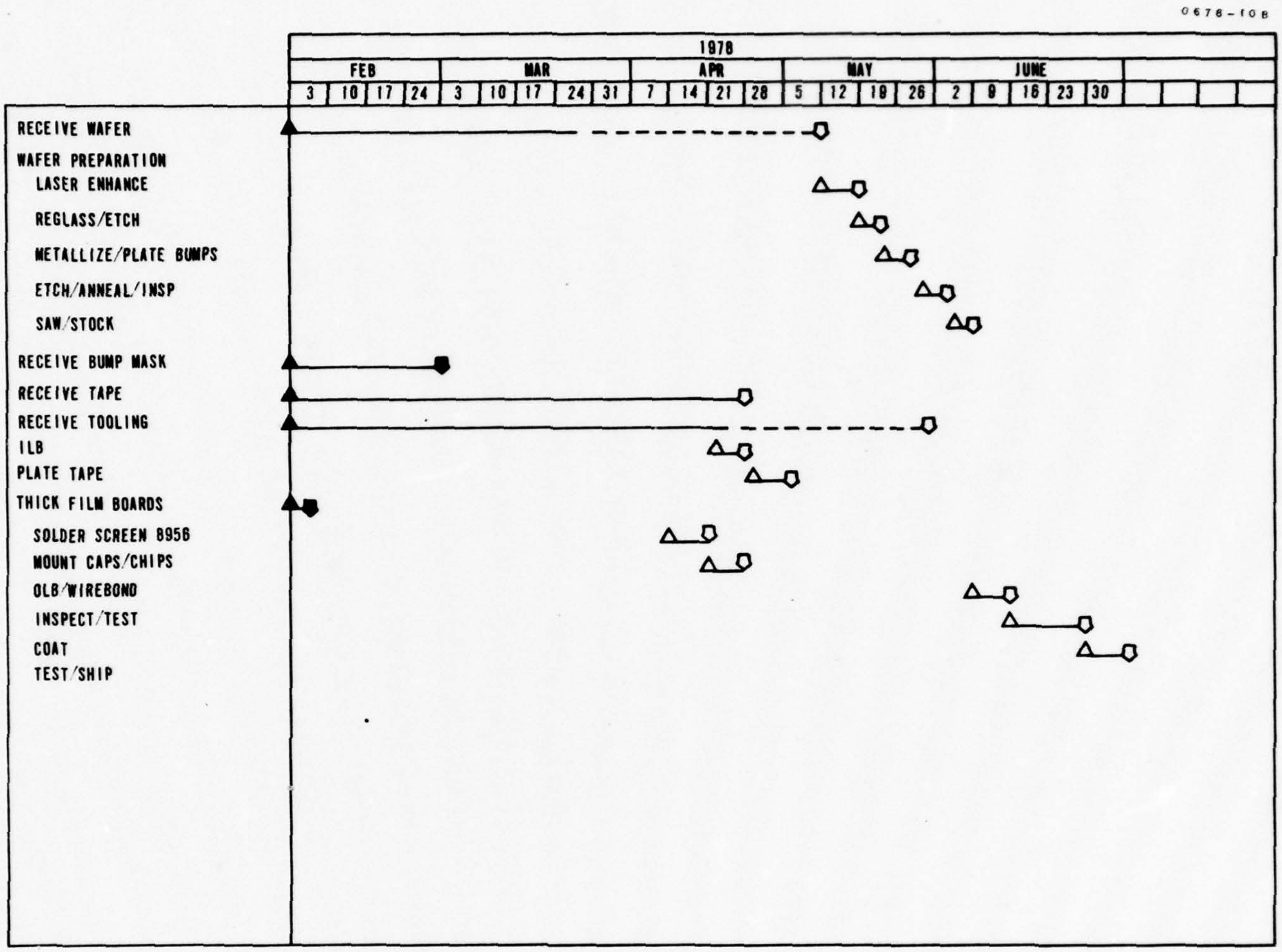


FIGURE 4-8. MANUFACTURING SCHEDULE - SECOND SUBMISSION - MINILASER RANGEFINDER

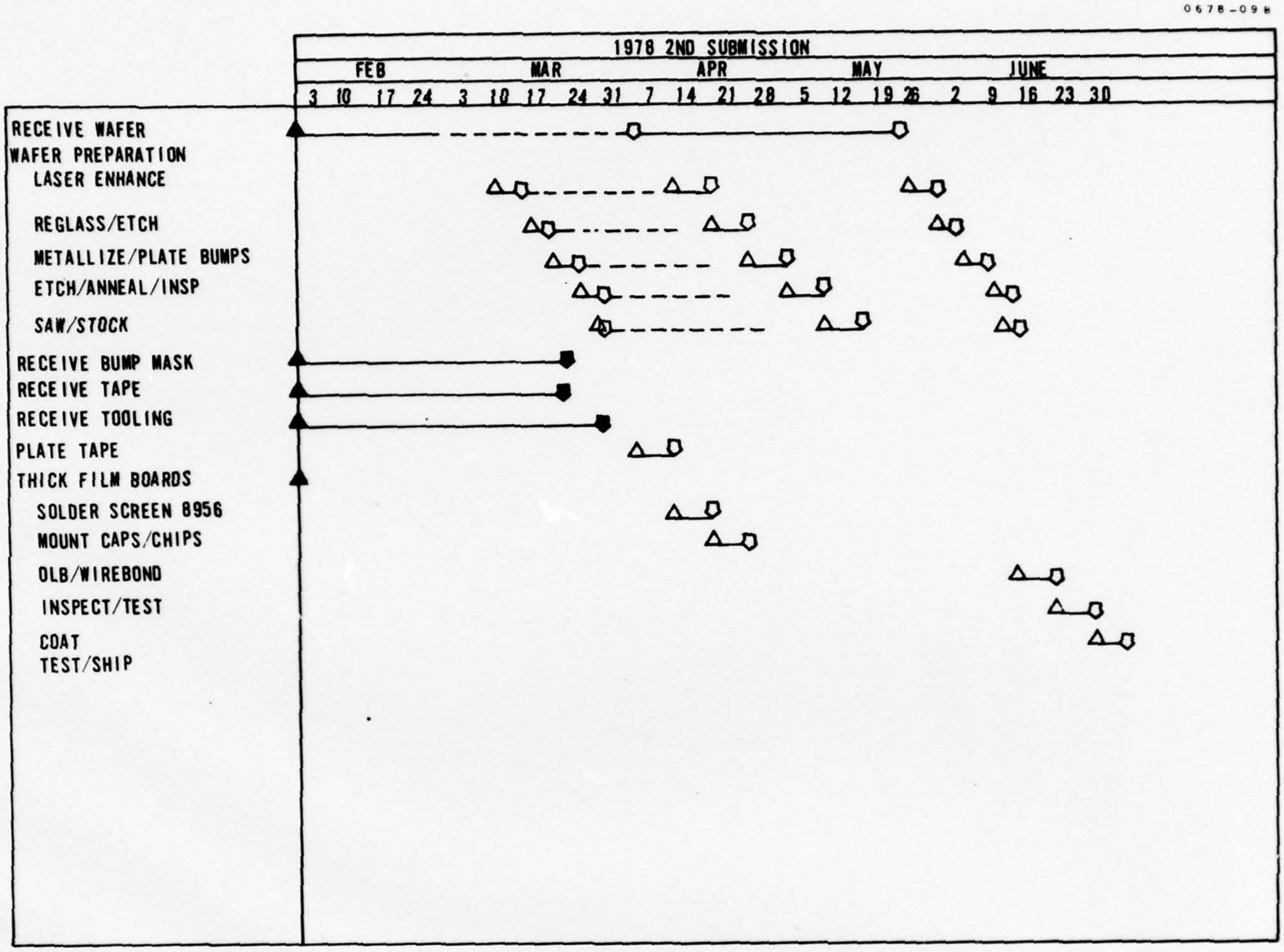


FIGURE 4-9. MANUFACTURING SCHEDULE - SECOND SUBMISSION - SINCGARS DISCRIMINATOR

Section 5

CONCLUSIONS

During this third reporting period good progress continued in most areas of the program. The Crystal Oscillator and Temperature Controller Circuits, now nearly completed, continued to require excessive effort. However, it is felt that the data generated on these devices is important and useful to ERADCOM. A major cost growth problem was identified and discussed with ERADCOM during this period. The work on the above mentioned devices and greater than estimated complexity of the Material Handling System contributed to the high costs. The program is now moving into the TCC phase with wafer bumping activities being initiated.

Section 6

PLANS FOR THE NEXT REPORTING PERIOD

During the next reporting period major emphasis will be placed on the TCC assembly operations for the second submission engineering samples. All device types will require extensive activity in wafer bumping, inner lead bonding testing and outer lead bonding. In the area of Material Handling the Air Substrate Feed Mechanism and the Furnace On-Loader will be completely operational. The Furnace Off-Load system will be nearing completion. Work on the Burn-In system will progress steadily with all major parts in the fabricating cycle.

Section 7

PUBLICATIONS

1. "Automated Tape Carrier Bonding for Hybrids" - by Dr. Rudolph G. Oswald, William R. Rodrigues de Miranda and James M. Montante - Solid State Technology magazine, March 1978, p. 39.

2. "Outer Lead Bonding Pattern Configurations for Tape Bonded Hybrids" by William R. Rodrigues de Miranda and Dr. Rudolph G. Oswald, Southeast Printed Circuits and Microelectronics Conference, Orlando, Florida - March 15, 1978.

APPENDIX A

Universal
Report No. ____________

Originator's
Report No. Discriminator -001

Revision ____________

REPORT OF TEST ON SINCGARS Discriminator - First Submission of Engineering Samples

CDRL B001

TEST PERFORMED BY:

HONEYWELL, INC.
AVIONICS DIVISION
ST. PETERSBURG, FLA. 33733

TEST AUTHORIZED BY:

ERADCOM
FT. MONMOUTH, NJ 07703
CONTRACT NO. DAAB07-77-C-0526

Universal
Report No. ____________________

Originator's
Report No. Discriminator -001

Revision ________

REPORT OF TEST ON SINCGARS Discriminator - First Submission of Engineering Samples

TEST PERFORMED BY:

HONEYWELL, INC.
AVIONICS DIVISION
ST. PETERSBURG, FLA. 33733

TEST AUTHORIZED BY:

ERADCOM
FT. MONMOUTH, NJ 07703
CONTRACT NO. DAAB07-77-C-0526

	Date	Signature	
Test Initiated	2/1/78		
Test Completed	2/1/78		
Report Written By	2/2/78	S. Jones S. Jones	
Technician			
Test Engineer			
Supervisor	2/3/78	W. Miranda R. Oswitch for W. Miranda	
Supervisor			
Government Repr. (if applicable)			
Final Release	2/3/78		

1.1 Reason for Test

Acceptance tests were performed on the first lot of engineering samples to be delivered to ECOM under Contract DAAB07-77-C-0526. The purpose of these tests is to demonstrate that these samples are functional and meet the specifications listed in paragraphs 1.3.2.1 through 1.3.2.6.

1.2 Description of Test Apparatus

The equipment listed below was used to perform the tests specified in paragraph 1.3. The Discriminator Manual Test Fixture is a special piece of test equipment built by Honeywell. This test fixture contains the switch and circuitry required to perform the tests specified in paragraph 1.3.2. Figure 1 shows the schematic of this fixture.

Equipment Used	Model #	HI ID #	Last Calibrated	Due For Calibration
Hewlett Packard Synthesized Signal Generator	8660B	30496	11/16/77	9/16/78
Hewlett Packard Modulation Section	86632A	30497	11/16/77	9/16/78
Hewlett Packard RF Section	86601A	30498	11/16/77	9/16/78
Tektronix Oscilloscope	475	CG11584	12/16/77	7/16/78
Fluke Digital Multimeter	8600A	CG13567	12/6/77	7/6/78
Ambitrol Twin Power Supply	TW5005	CG1804-37	11/4/77	11/4/78
Hewlett Packard Distortion Analyzer	334A	30727	9/28/77	1/28/79
Exact Signal Generator	7060	CG11351	6/24/77	3/24/78
Discriminator Test Fixture	N/A	N/A	N/A	N/A

NOTE: The power supply output level was set with the aid of the Fluke Digital Multimeter.

1.3 Test Procedure

1.3.1 Test Circuit

The test configuration for conducting the tests specified in paragraph 1.3.2 is illustrated in Figure 1.

1.3.2 Electrical Requirements

1.3.2.1 Audio Output Voltage

With the HP 8660 and associated equipment set up for 1KHz modulation, 300 uV IF output and a deviation of 5 KHz, the audio output at pins 1 to 2/3 shall be greater than 40 mV.

1.3.2.2 Total Harmonic Distortion

With the HP 8660 and associated equipment set up for 1 KHz modulation, 300 uV IF output and a deviation of 8 KHz, the total harmonic distortion of the audio output at pins 1 to 2/3 shall be less than 5 percent.

1.3.2.3 Audio Output Due to Decrease of IF Input

With the same input conditions as specified in paragraph 1.3.2.2, decrease the IF input until the amplitude of the audio output (pins 1 to 2/3) decreases by 3 dB. The IF input shall be less than 200 uV as read on the meter located on the RF Section of the HP 8660.

1.3.2.4 Audio Output Due to Decreasing AGC

With the HP 8660 and associated equipment set up for 1 KHz modulation, 32 mV IF output and a deviation of 8 KHz, adjust the AGC control on the Discriminator test fixture (see Figure 1) counterclockwise until the amplitude of the audio output decreases by 3 dB. The voltage at pin 7 shall be greater than 2.5 Vdc.

1.3.2.5 Input Current

With the same input conditions as specified in paragraph 1.3.2.2, the current into pins 5 and 6 shall be less than 7.5 mA.

1.3.2.6 Output Filter Bandpass

With the same input conditions as specified in paragraph 1.3.2.2 except that an external oscillator is used for modulation (Exact 7060), measure the upper and lower 3dB frequency limits of the Discriminator output. The lower limit shall be less than 5 Hz and the upper limit shall be greater than 25kHz. The Discriminator output at 100KHz modulation shall not be more than -24dB down from the output with 1 kHz modulation.

1.4 Test Data

The five engineering samples being delivered passed all functional tests. Test data sheets which contain the test results for Serial Numbers 7, 8, 9 10 and 11 are attached.

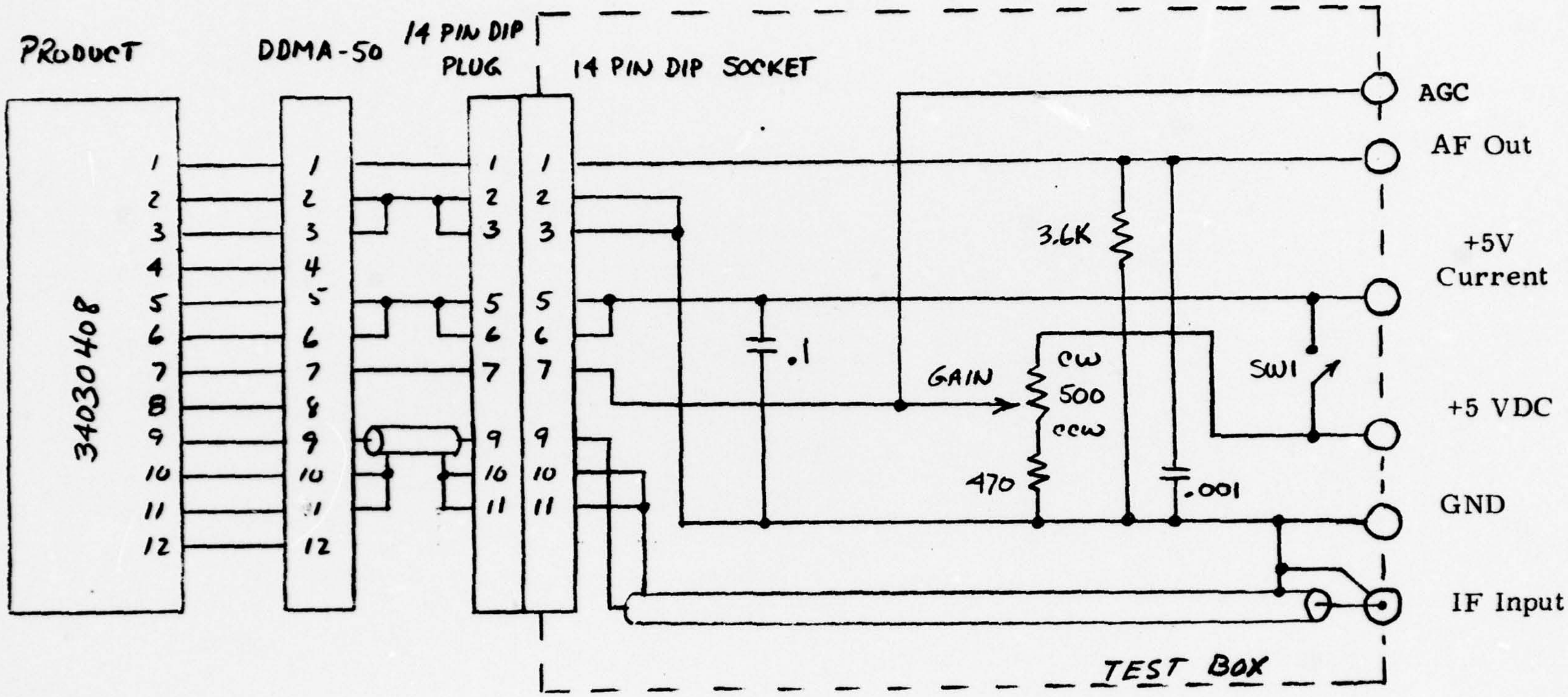


FIGURE 1 - DISCRIMINATOR TEST FIXTURE

DISCRIMINATOR
P/N 34030408-001

S/N 7
Date 2-1-78

1. Audio Output Voltage

63 mV

> 40mV

2. Total Harmonic Distortion

1.7 %

< 5 percent

3. Audio Output -3dB (due to decrease of IF input)

90 μV

IF Input Voltage < 200μV

4. Audio Output -3dB (due to decreasing AGC control)

3.55 V

Voltage @ Pin 7 > 2.5V

5. Input Current (Pins 5 & 6)

3.94 mA

< 7.5mA

6. Output Filter Bandpass

(a) Lower -3dB Frequency

3.1 Hz

< 5Hz

(b) Upper -3dB Frequency

30 kHz

> 25 kHz

(c) At 100kHz

-21.0 dB

-24dB max.

DISCRIMINATOR
P/N 34030408-001

S/N 8
Date 2-1-78

1. Audio Output Voltage

56 mV
$> 40mV$

2. Total Harmonic Distortion

2.8 %
< 5 percent

3. Audio Output -3dB (due to decrease of IF input)

90 μV
IF Input Voltage $< 200\mu V$

4. Audio Output -3dB (due to decreasing AGC control)

3.38V
Voltage @ Pin 7 $> 2.5V$

5. Input Current (Pins 5 & 6)

3.93 mA
$< 7.5mA$

6. Output Filter Bandpass

(a) Lower -3dB Frequency

3.4 Hz
$< 5Hz$

(b) Upper -3dB Frequency

28.4kHz
> 25 kHz

(c) At 100kHz

-21.0 dB
-24dB max.

DISCRIMINATOR
P/N 34030408-001

S/N 9
Date 2-1-78

1. Audio Output Voltage

44 mV
> 40mV

2. Total Harmonic Distortion

3.8%
< 5 percent

3. Audio Output -3dB (due to decrease of IF input)

150 μV
IF Input Voltage < 200μV

4. Audio Output -3dB (due to decreasing AGC control)

3.60 V
Voltage @ Pin 7 > 2.5V

5. Input Current (Pins 5 & 6)

3.99 mA
< 7.5mA

6. Output Filter Bandpass

(a) Lower -3dB Frequency

3.4 Hz
< 5Hz

(b) Upper -3dB Frequency

38.4 kHz
> 25 kHz

(c) At 100kHz

-18.9 dB
-24dB max.

DISCRIMINATOR
P/N 34030408-001

S/N 10
Date 2-1-78

1. Audio Output Voltage

59 mV
$> 40mV$

2. Total Harmonic Distortion

1.8 %
< 5 percent

3. Audio Output -3dB (due to decrease of IF input)

80 µV
IF Input Voltage $< 200 \mu V$

4. Audio Output -3dB (due to decreasing AGC control)

3.32 V
Voltage @ Pin 7 $> 2.5V$

5. Input Current (Pins 5 & 6)

4.06 mA
$< 7.5mA$

6. Output Filter Bandpass

(a) Lower -3dB Frequency

3.4 Hz
$< 5Hz$

(b) Upper -3dB Frequency

27.8 kHz
> 25 kHz

(c) At 100kHz

-22.0 dB
-24dB max.

DISCRIMINATOR
P/N 34030408-001

S/N 11
Date 2-1-78

1. Audio Output Voltage

64 mV
> 40mV

2. Total Harmonic Distortion

2.1 %
< 5 percent

3. Audio Output -3dB (due to decrease of IF input)

110 μV
IF Input Voltage < 200μV

4. Audio Output -3dB (due to decreasing AGC control)

3.44 V
Voltage @ Pin 7 > 2.5V

5. Input Current (Pins 5 & 6)

4.12 mA
< 7.5mA

6. Output Filter Bandpass

(a) Lower -3dB Frequency

3.5 Hz
< 5Hz

(b) Upper -3dB Frequency

32.0 kHz
> 25 kHz

(c) At 100kHz

-20.4 dB
-24dB max.

DISTRIBUTION LIST

Commander Defense Documentation Center Attn: DDC-TCA Cameron Station, Building 5 Alexandria, VA 22314	12
Office of Defense Research & Engineering Communications and Electronics Room 3D1037 Washington, DC 20330	1
Director US Army Production Equipment Agency Attn: Mr. C. McBurney Rock Island Arsenal Rock Island, IL 61201	1
Department of Defense Deputy for Science & Technology Ofc Assist Sec Army (R&D) Washington, DC 20310	1
Advisory Group on Electron Devices 201 Varick Street, 9th Floor New York, NY 10014	2
Chief, Research & Development Attn: Director of Developments Department of the Army Washington, DC 20310	1
Commander US Army Research Office Attn: DRXRO-IP PO Box 12211 Research Triangle Park, NC 27709	1
Commander US Army Missile Command Redstone Scientific Info Center Attn: Chief, Document Section Redstone Arsenal, AL 35809	1
US Army Missile Command Attn: DRSMI-RGP (Mr. Victor Ruwe) Redstone Arsenal, AL 35805	1
Commander Harry Diamond Laboratories Attn: Mr. Horst Gerlach (DRXDO-RAA) 2800 Powder Mill Road Adelphia, MD 20783	1
Commander Naval Electronics Laboratory Center Attn: Library San Diego, CA 92152	1
Commander Department of the Navy, Elex 05143A Attn: A.H. Young Electronics System Command Washington, DC 20360	1
Chief Naval Ship Systems Command Department of the Navy Attn: Code 681A2b, Mr. L. Gumina Room 3329 Washington, DC	1
Commander US Naval Air Development Center Attn: Library Johnsville, Warminster, PA 18974	2
Commander Naval Ocean Systems Command Attn: Mr. Richard Gamble San Diego, CA 92152	1

Distribution List

Commander 1
Air Research & Development Command
Attn: RDTCT
Andrews Air Force Base
Washington, DC

Commander 1
Rome Air Development Center
Griffiss Air Force Base
Attn: (EMERR) Mr. L. Gubbins
Rome, NY 13440

Commander 1
Air Force Materials Laboratory
Attn: MATE (Ms. E. Torrance)
Electronic Branch
Wright-Patterson Air Force Base
Dayton, Ohio 45433

Commander 1
Rome Air Development Center
Griffiss Air Force Base
Attn: (EMERR) Mr. Regis C. Hilow
Rome, NY 13440

AFAL (AVTA) 1
Electronic Technology Division
Attn: Mr. Robert D. Larson, Chief
Advanced Electronics Devices Branch
Wright-Patterson Air Force Base
Dayton, Ohio 45433

NASA Scientific & Tech 2
Information Facility
PO Box 8757
Baltimore/Washington Int'l Airport
Baltimore, MD 21240

National Aeronautics & Space 1
Administration
George C. Marshall Space Flight Center
Attn: R-QUAL-FP (Mr. Leon C. Hamiter)
Huntsville, AL 35812

NSSA Manned Space Craft Center 1
Reliability and Flight Safety
Division
Attn: Library
Houston, TX 77002

Alpha Industries, Inc. 1
20 Sylvan Road
Woburn, MA 08101

AVANTEK 1
Attn: Mr. Thielan
3001 Copper Road
Santa Clara, CA 95051

Amelco Semiconductor 1
PO Box 1030
Mountain View, CA 94042

Bell Laboratories 1
Whippany Road
Attn: Tech Reports Center
WH5E-227
Whippany, NJ 07981

Philco Ford 1
Attn: Mr. D. Heiden
Landsdale, PA

General Instrument Corp 1
Semiconductor Products Group
600 West John Street
Hicksville, Long Island, NY 11802

Hughes Aircraft Corporation 1
Attn: Dr. Bruce Gammer
3100 West Lmita Boulevard
Torrance, CA 90509

Hughes Aircraft Corporation 1
Attn: Mr. D. Hartman
Bldg 100 MSA788
PO Box 90515
Los Angeles, CA 90009

Hughes Aircraft Company 1
Microelectronics Laboratory
500 Superior Avenue
Newport Beach, CA 92663

Honeywell Inc. 1
Semiconductor Products
2747 Fourth Avenue
Minneapolis, MN 55408

Distribution List

Harris Semiconductor 1
PO Box 883
Melbourne, FL 32901

IBM 1
Components Division
Attn: Mr. Al Kran
East Fishkill, Rt. 52
Hopewell Junction, NY 12533

KSC Semiconductor Corp 1
Attn: Mr. S. Cudletz, President
KSC Way (Katrina Road)
Chelmsford, MA 01824

Arthur D. Little 1
Acorn Park
Attn: Dr. H. Rudenberg 15/206
Cambridge, MA 02140

Motorola, Inc. 1
Attn: Mr. J. LaRue
5005 East McDowell Road
Phoenix, AZ 85008

Dr. Robert H. Rediker 1
Massachusetts Institute of Technology
Building 13-3050
Cambridge, MA 02139

Microwave Associates 1
Attn: Dr. F. Brand
Burlington, MA 01803

Rockwell International 1
Collins Radio Group
Attn: Dr. Cheng Wen
MS 406-246
Dallas, TX 75207

Northrop Corporation Laboratories 1
Attn: Library 320-61
3401 West Broadway
Hawthorne, CA 90250

Rockwell International 1
Corporation Science Center
Thousand Oaks, CA

Raytheon Company 1
Semiconductor Operation
Attn: Mr. S. Weinsner
350 Ellis Street
Mountain View, CA 94040

Raytheon Company 1
Attn: Dr. S. F. Paik
130 Second Avenue
Waltham, MA 02154

Sanders Associates, Inc. 1
Attn: Microwave Department
95 Canal Street
Nashua, NH 03060

TRW Semiconductor Inc. 1
Attn: Mr. B. Lindgren
14520 Aviation Blvd
Lawndale, CA 90260

Texas Instruments 1
Attn: Technical Reports Service
PO Box 5936, MS 105
Dallas, TX 75222

Commander
US Army Electronics R&D Command
Fort Monmouth, NJ 07703

DELEW-D	1
DELCS-D	1
DELAS-D	1
DELSD-AS	1
DELET-DD	1
DELET-DT	2
DELET-I	3
DELET-IT	9
DELET-P	1
DELSD-L (Tech Library)	1
DELSD-D	1
DELET-D	1
DELSD-L-S-2 cys	2